US 20020101547A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0101547 A1

LEE et al. (43) Pub. Date: Aug. 1, 2002

(54) LIQUID CRYSTAL DISPLAYS

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(*) Notice: This is a publication of a continued prosecution application (CPA) filed under 37 CFR 1.53(d).

(21) Appl. No.: 09/172,130

(22) Filed: Oct. 14, 1998

Publication Classification

(51) Int. Cl.[7] G02F 1/1333

(52) U.S. Cl. 349/40

(57) ABSTRACT

A data line and an amorphous silicon pattern are formed on a substrate. The first electrode pattern is extended from the data line and overlaps an edge of the amorphous silicon pattern. The second electrode pattern is made of the same metal as the first electrode pattern and overlaps the edge of the amorphous silicon pattern at an opposite side of the first electrode pattern. Edges of the first and the second electrode patterns are sharply formed so that a tunneling effect easily occurs through the amorphous silicon pattern. An indium-tin-oxide pattern for a capacitor is formed at the end of the second electrode pattern. The capacitor is formed between the ITO pattern and a common electrode.

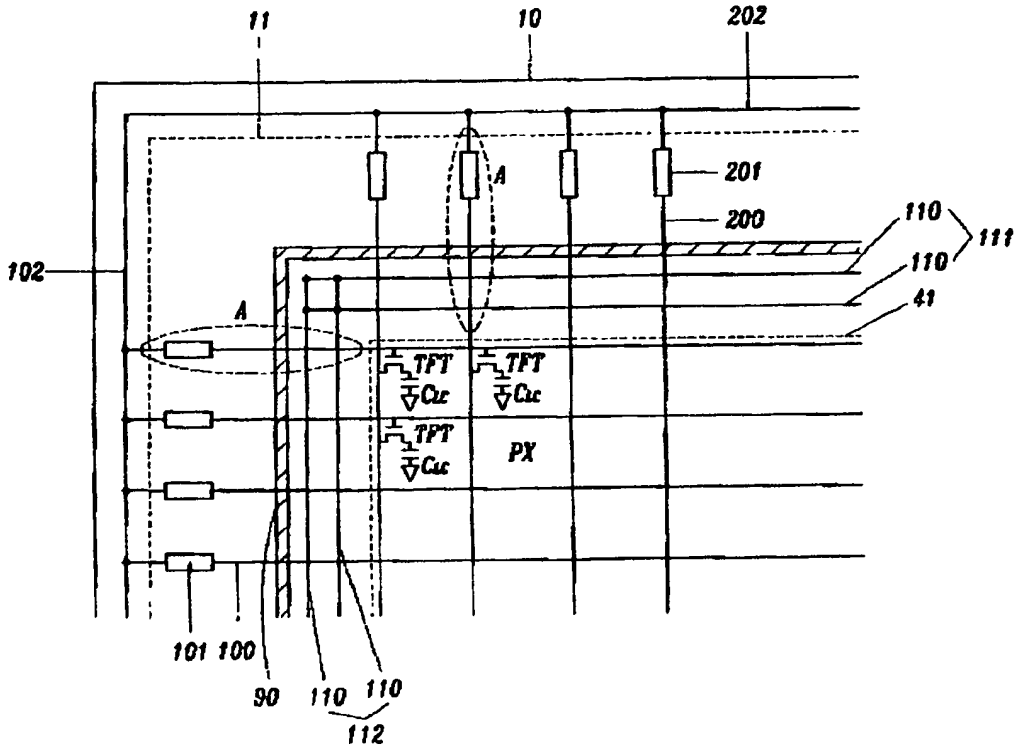


FIG.1 (Prior Art)

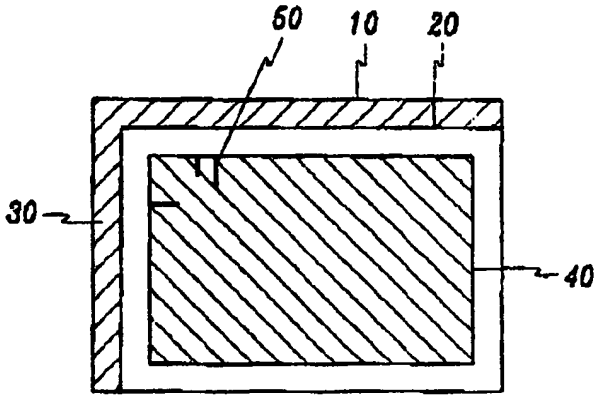
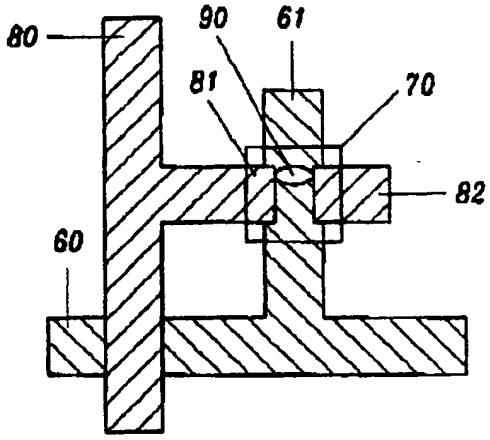
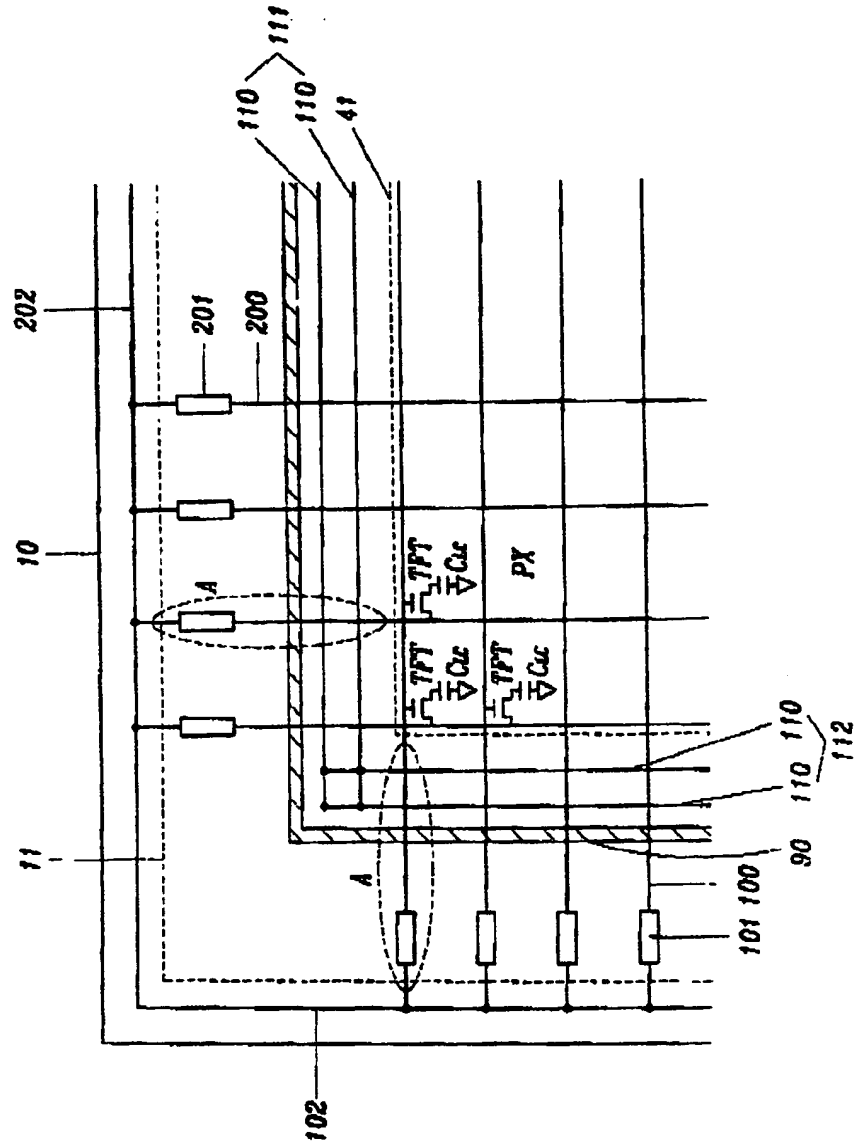


FIG.2 (Prior Art)

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110
41
202
201
200
10
A
TFT
Cst
PX
TFT
Cst
TFT
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11
90
A
100
101
102

FIG.3

FIG.5

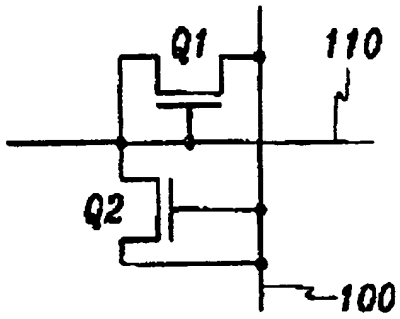
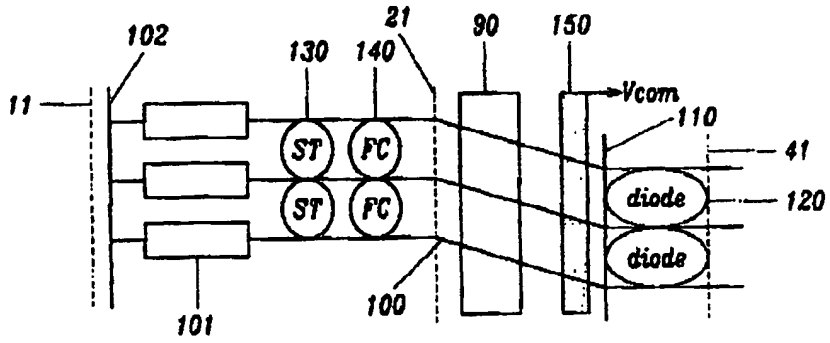


FIG.4


102
130
140
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150
Vcom
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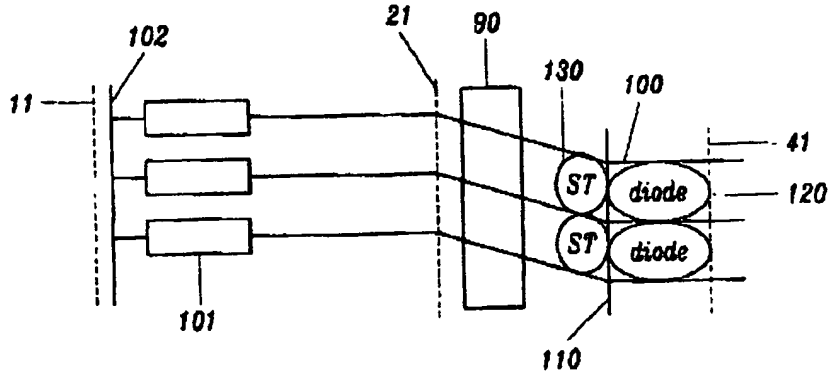
ST
FC
ST
FC
41
diode
120
diode
101
100

FIG.6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11
41
ST
diode
120
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101
110

FIG.7

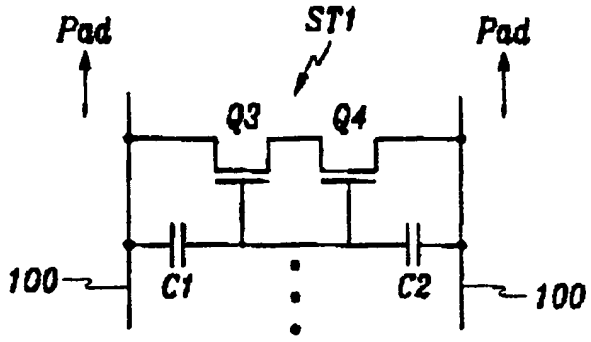


FIG.8

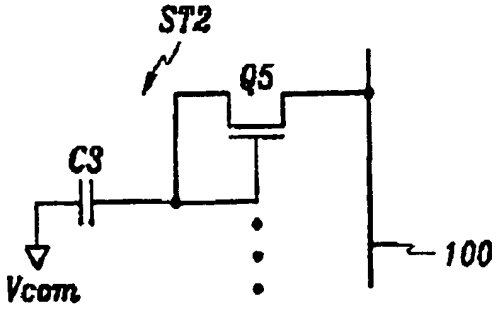


FIG.9

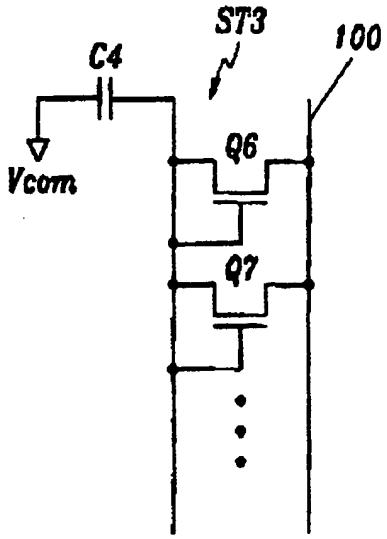


FIG.10

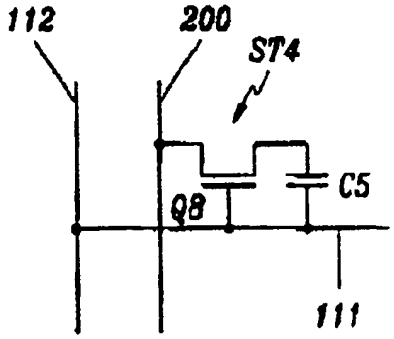


FIG. 11

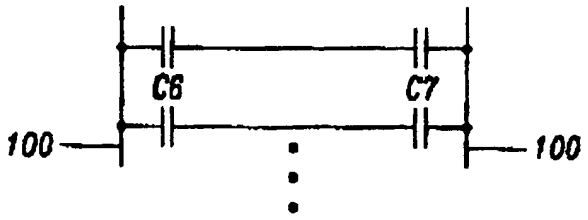
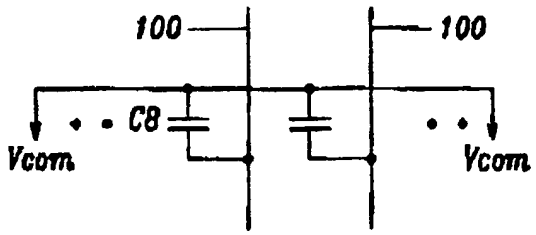


FIG. 12



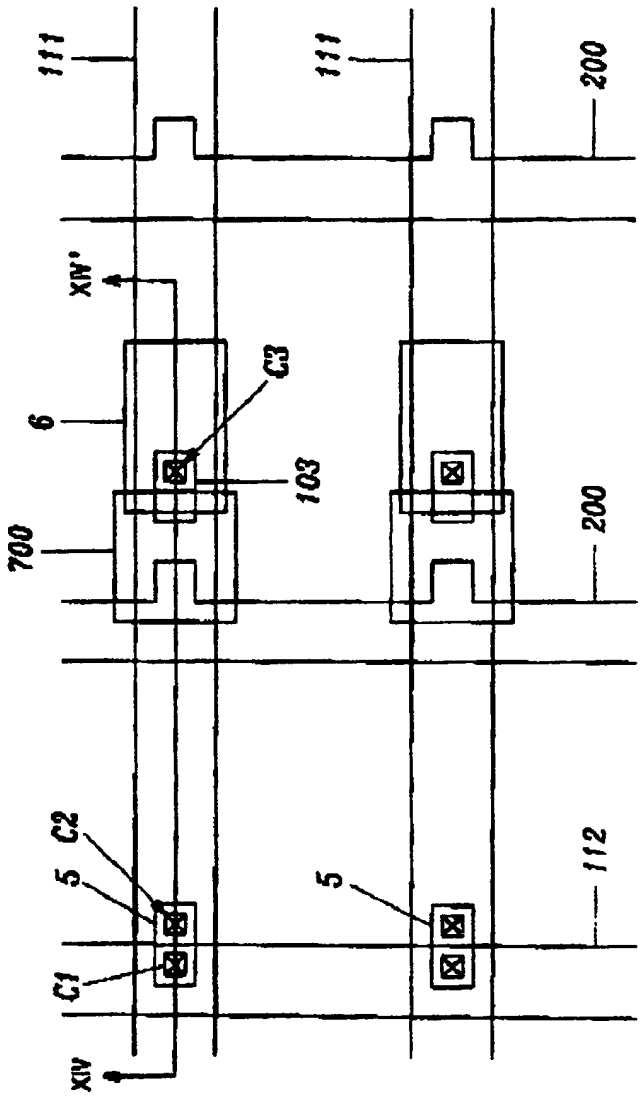
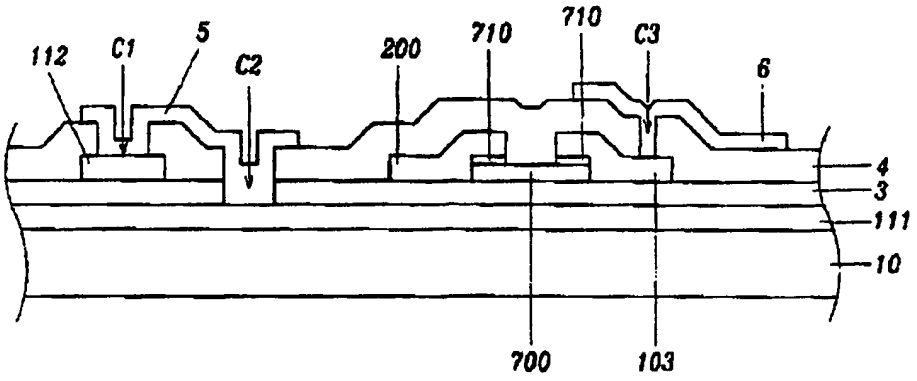


FIG.13

FIG.14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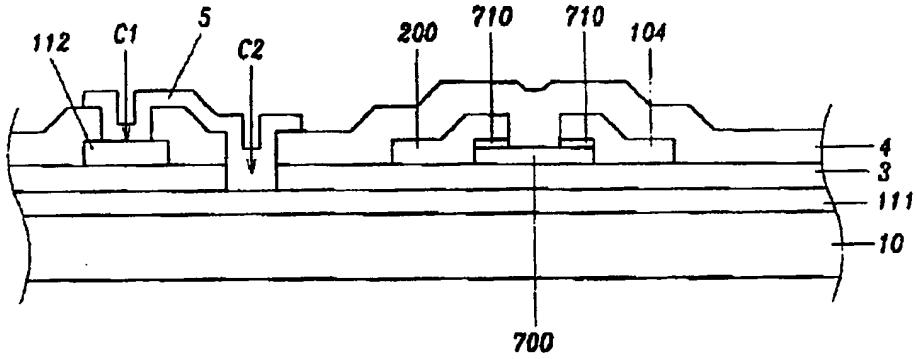
C1
5
C2
200
710
710
C3
6
4
3
111
10
700
103

FIG.16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C1
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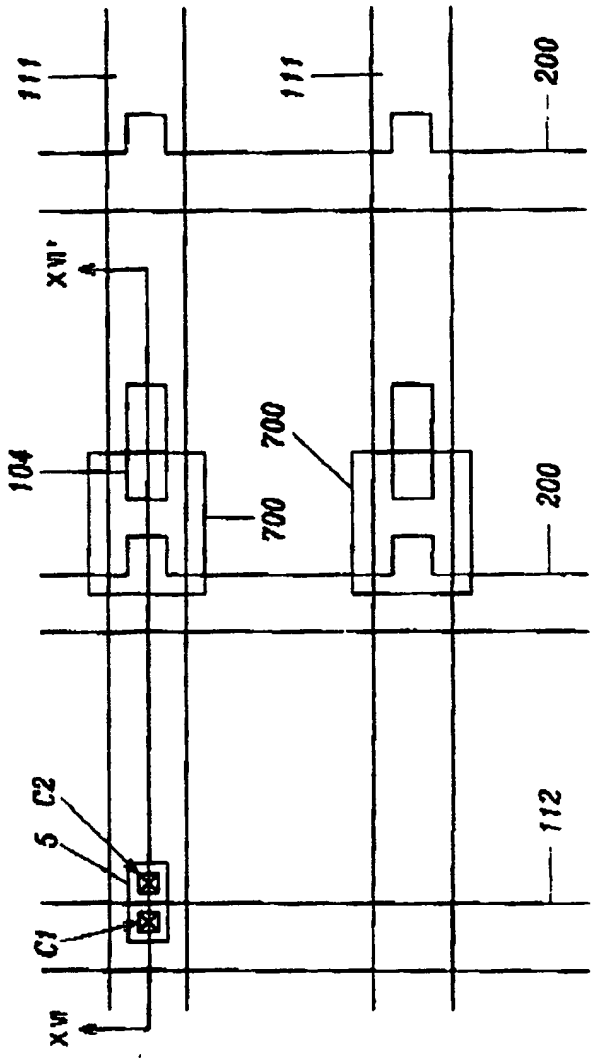


FIG.15

FIG. 17

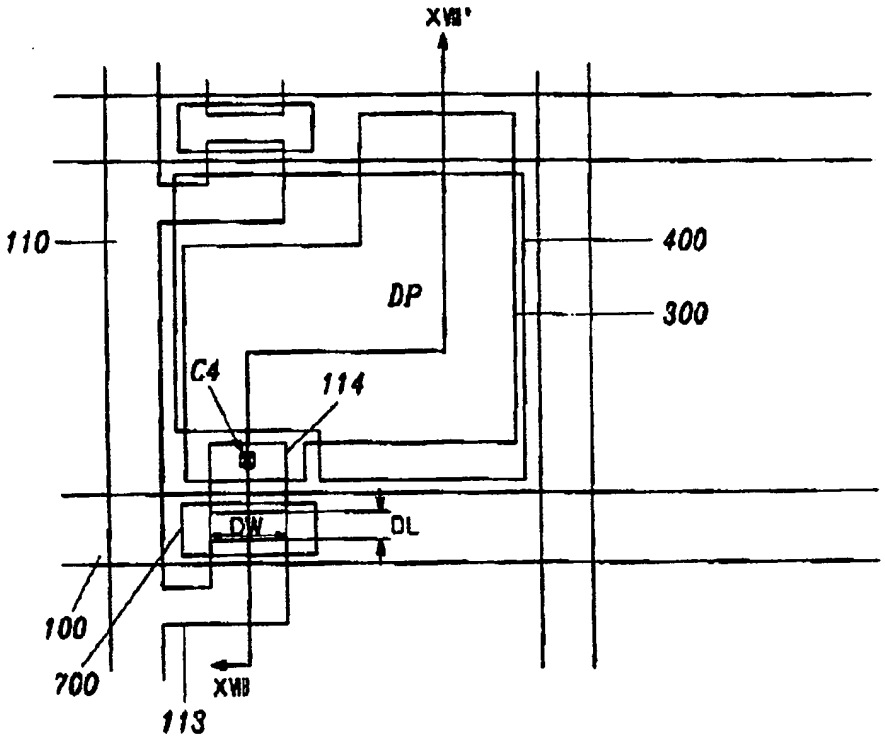


FIG.18

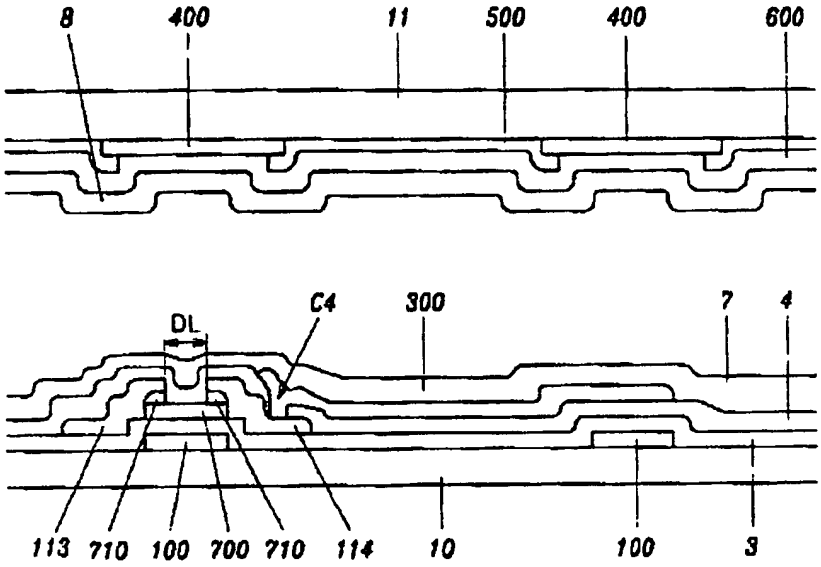
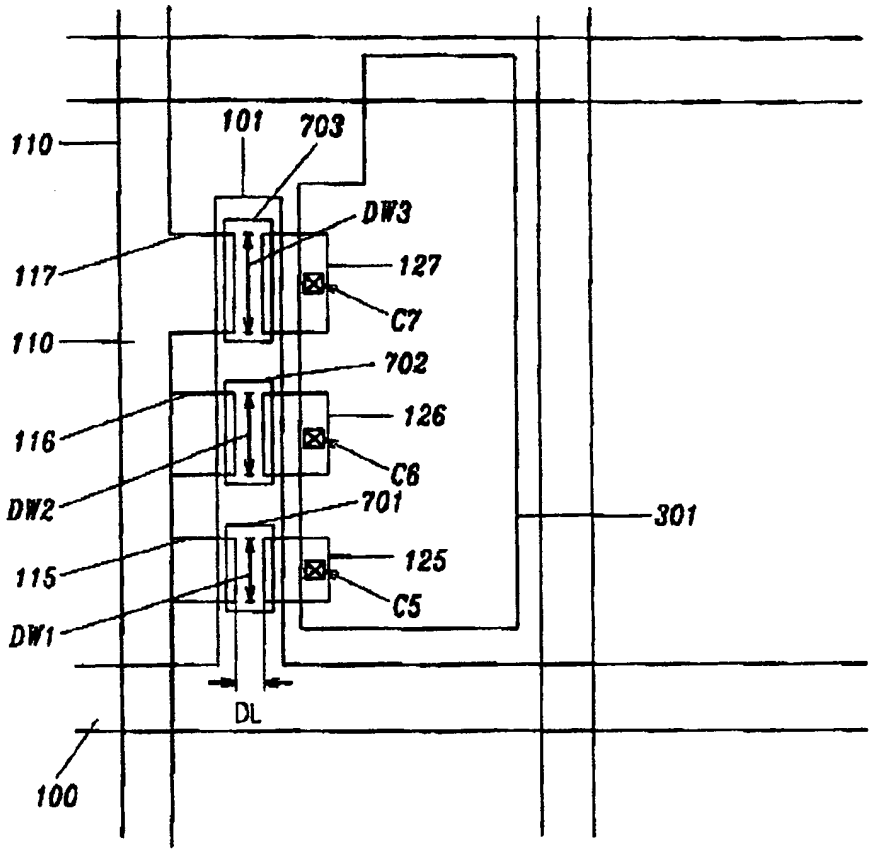


FIG. 19


101
703
110
DW3
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C7
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702
116
126
C6
DW2
701
301
115
125
C5
DW1
DL
100

FIG.20

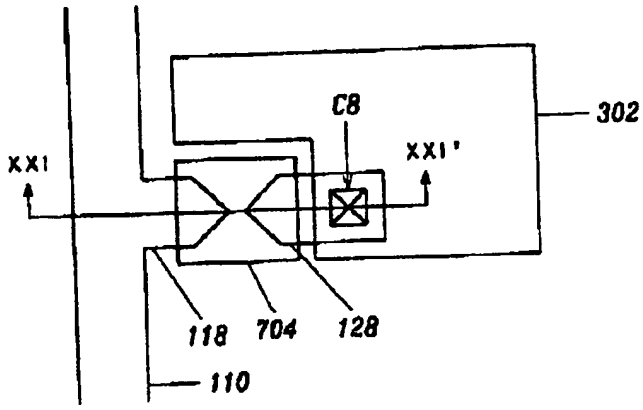
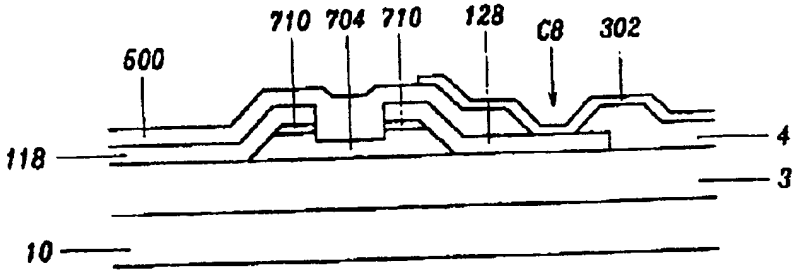

C8
302
XX1
XX1'
118
704
128
110

FIG.21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704
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128
C8
302
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4
118
3
10

FIG.22

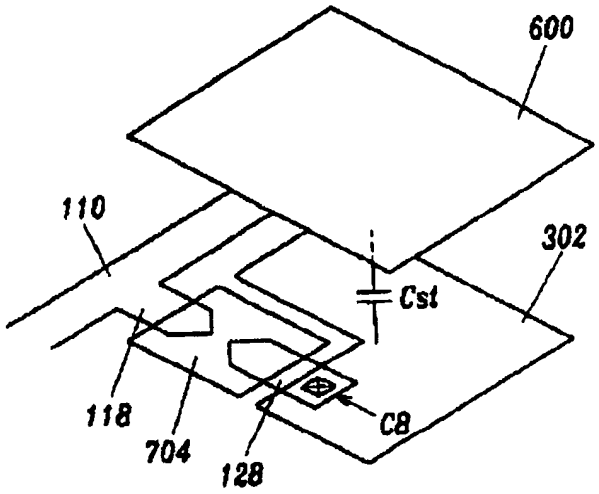


FIG.23

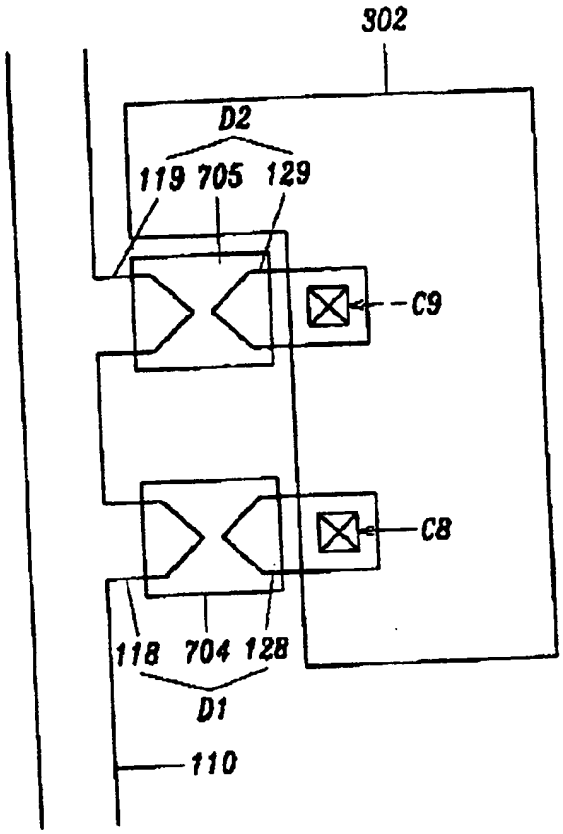


FIG.24

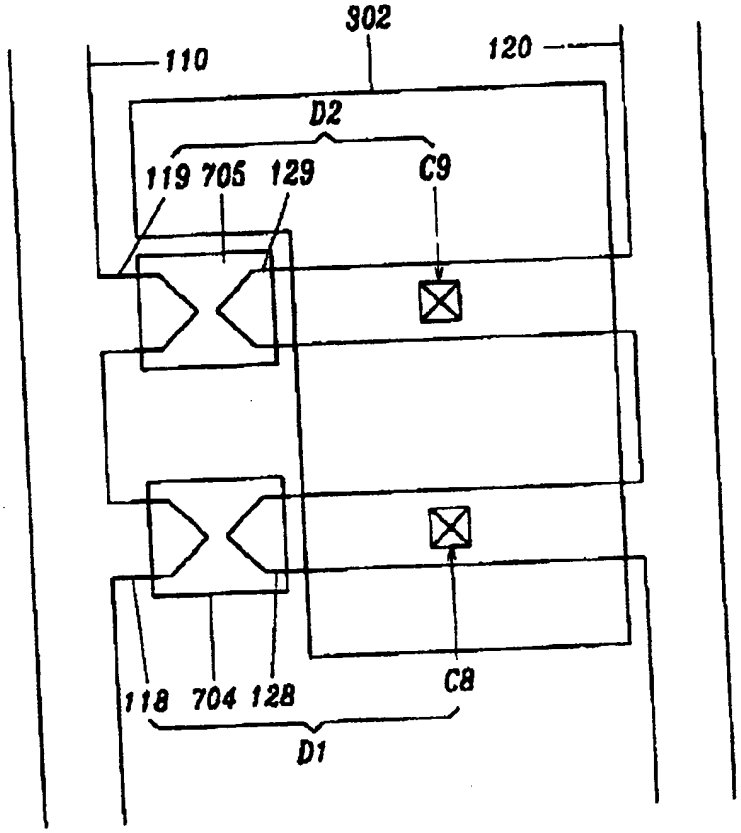


FIG.25

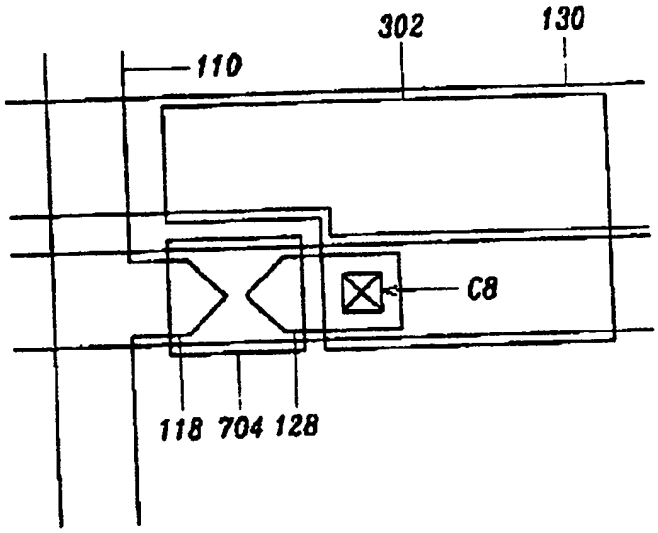


FIG.26A

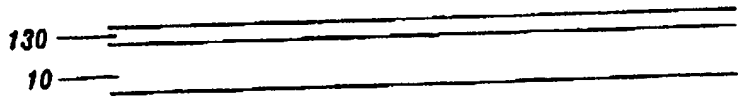


FIG.26B

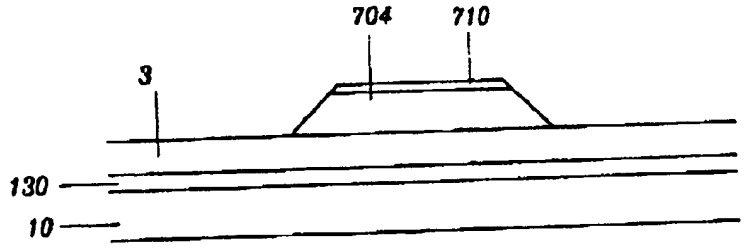


FIG.26C

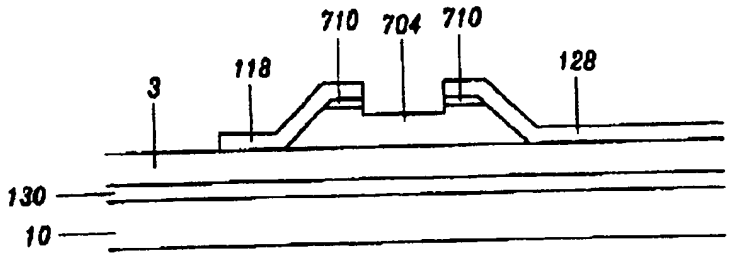


FIG.26D

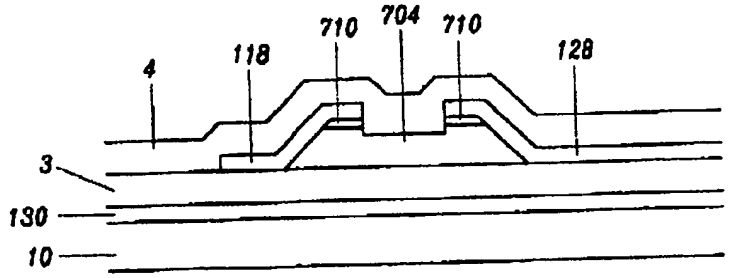


FIG.26E

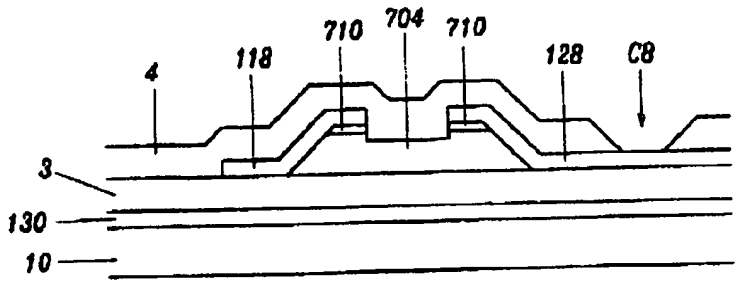


FIG.26F

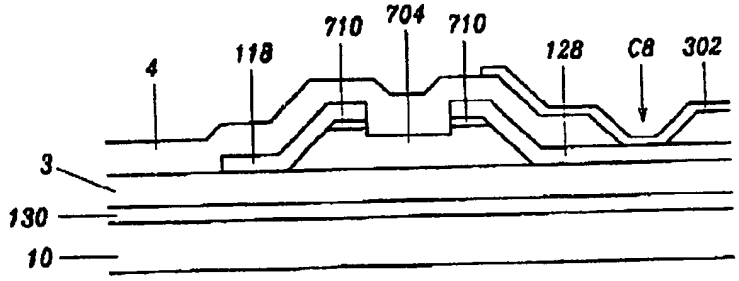


FIG.27

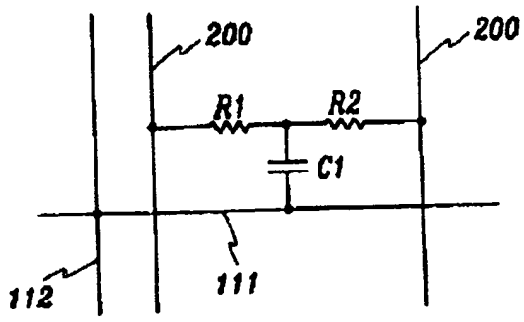


FIG.28

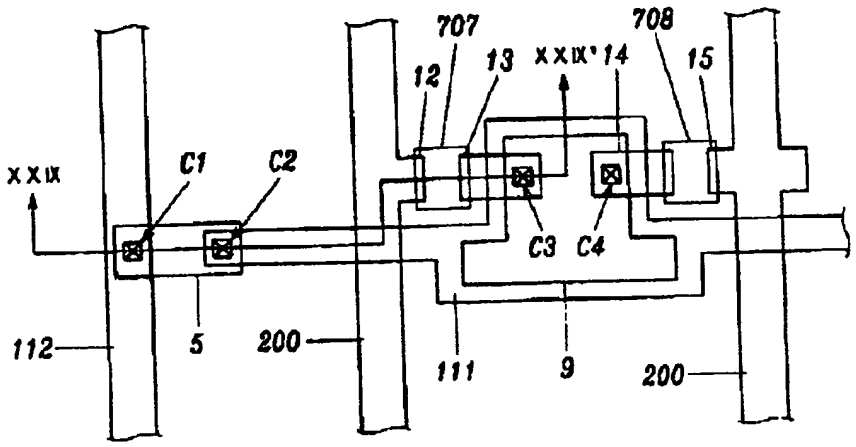


FIG.29

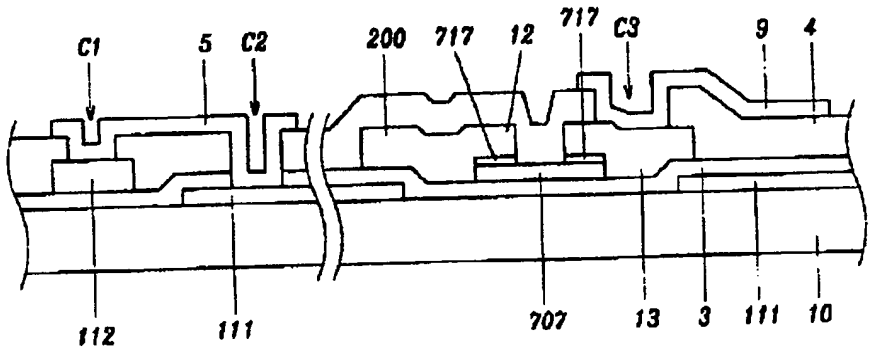


FIG.30

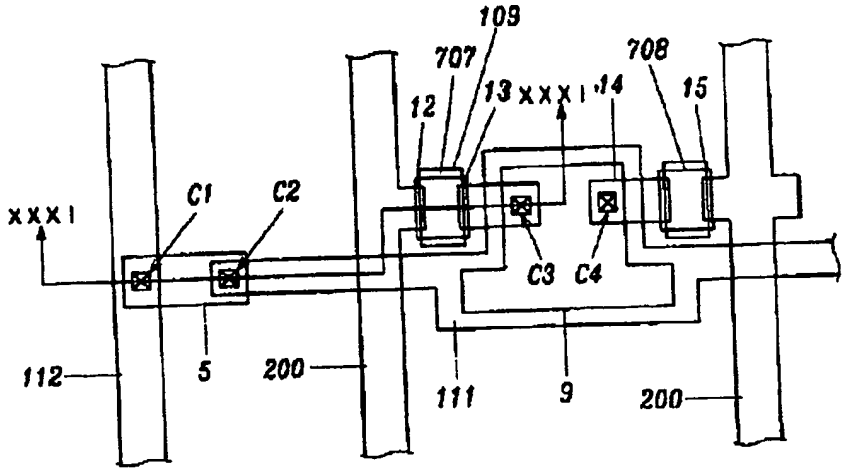


FIG.31

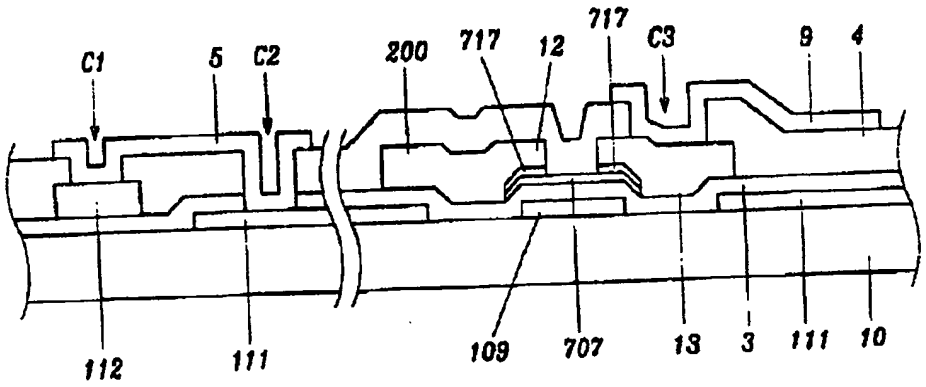


FIG.32

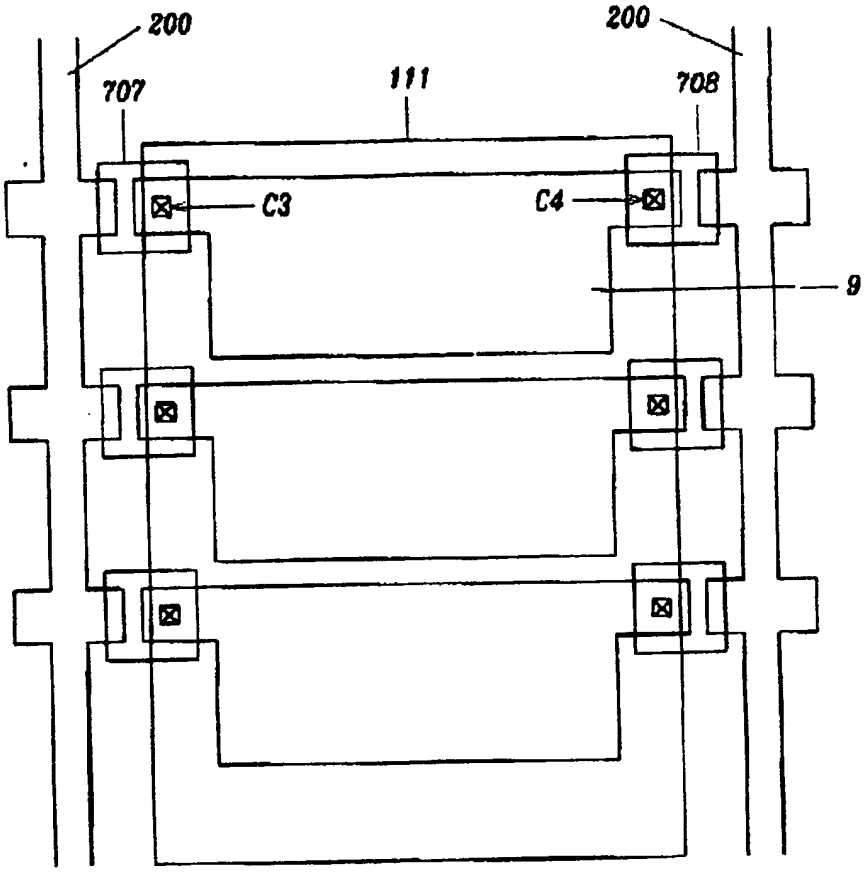


FIG.33

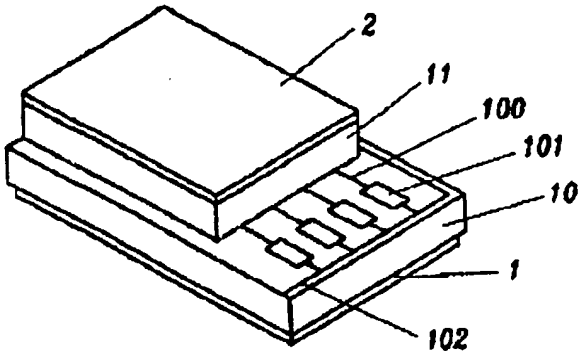
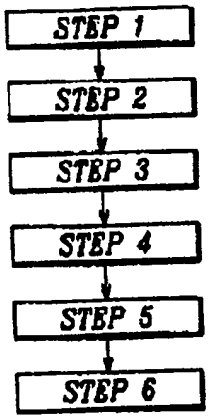


FIG.34



LIQUID CRYSTAL DISPLAYS

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to liquid crystal displays (referred to as an LCD hereinafter) and manufacturing methods thereof, and more particularly, to circuits for preventing electrostatic discharge which are provided in the LCD and manufacturing methods thereof.

[0003] (b) Description of the Related Art

[0004] A liquid crystal display (LCD), which is one type of flat panel display (FPD), includes two substrates having transparent electrodes and a liquid crystal layer interposed between the substrates. In the LCD, light transmittance is controlled by varying the voltages applied to the liquid crystal layer.

[0005] On a thin film transistor (TFT) substrate of the LCO, N gate lines and M data lines, which cross each other, define a plurality of pixels in an NxM matrix. A pixel electrode is formed in each of the pixels and the pixel electrode is connected to the gate and the data lines through a switching device such as the TFT. The TFT controls display signals transmitted through the data line according to the states of the scanning signals transmitted through the gate line

[0006] The majority of the LCD manufacturing process is performed on a glass substrate. Since the glass substrate is nonconductive, electric charges, which are abruptly generated on the substrate, cannot be dispersed. This may cause the insulating films or TFTs to become damaged by the electrostatic discharge.

[0007] In the LCD manufacturing process, since the electrostatic charges, which is generated after the step of assembling the TFT substrate and a color filter substrate is completed, cause high voltages even though the amount of the charges are small, the quality of the substrate decreases. In addition, since the electrostatic charge is usually generated during the step of cutting the substrate. then flow into an active area having the pixel regions through gate and data pads, the channels of the TFTs near the pads become damaged by the electrostatic discharge with easy.

[0008] **FIG. 1** shows a layout view of the conventional LCD substrate which is damaged by an electrostatic discharge. As shown in the drawing, the LCD panel includes a TFT substrate **10** and a color filter substrate **20**. A pad area **30**, in which pads are formed to connect each wire of the TFT substrate **10** to driving circuits, and an active area **40**, in which actual images are displayed, are separately formed on the TFT substrate **10**.

[0009] Lines **50** in the active area **40** illustrate pixels having some defects by damaged TFT portions. If electrostatic charges are generated in the pad area **30** and moves inside the active area **40**, the channels of the TFTs, which are located near the pads, become damaged, or the quality of the channels is deteriorated.

[0010] The deteriorated TFT is shown in **FIG. 2**. As shown in the drawing, a gate line **60** and a data line **80** cross each other, and an edge of a gate electrode **61**, extended from the gate line **60**, overlaps an end of a source electrode **81** which is extended from the data line **80**. An edge of the gate electrode **61**, opposite the edge overlapping with the source electrode **81**, overlaps with a drain electrode **82**. A semiconductor film **70** is formed on the overlapping portion of the gate electrode **61**, source electrode **81** and drain electrode **82**.

[0011] If the electrostatic charges enter into the TFT, comprised of the semiconductor film **70**, the source and drain electrodes **81** and **82**, and the gate electrode **61**, sparks occur between the source and the drain electrodes **81** and **82**, thereby damaging the semiconductor film **70**.

[0012] To limit to the LCD by electrostatic discharge, a shorting bar, through which all metal wires are connected, is widely used for dispersing the electrostatic charges. However, in the case where an amount of the electric charges is large, it is not possible to completely prevent damage caused by the electrostatic discharge. Moreover, after the shorting bar is removed, it is not possible to prevent the electrostatic charges from entering into the substrate.

[0013] In manufacturing the LCD panel having the above structure, polarizers are attached after performing a visual display test by applying test signals to the shorting bar. Next, the main substrate is cut into individual LCO substrates, a liquid crystal material is injected between the substrates. and the injection holes are sealed. The shorting bar is removed in the step of cutting the substrate. In another visual display test, different test signals are applied to adjacent data lines by using probes directly contacted to each of the pads, then driving circuits are attached to the LCD panel.

[0014] As mentioned above, since the shorting bar is removed in the same step of cutting the substrate. it is difficult to protect the substrate against the electrostatic charges after the step of removing the shorting bar. Moreover, since the polarizers are attached after the simple test, in which only one signal is applied to every wire, by using the shorting bar, there is a high possibility that the polarizers are attached even on the damaged LCD panel. If the damaged panel is detected in the post-test, the panel, along with the expensive polarizers has to be discarded, thereby increasing overall manufacturing costs of the LCD.

SUMMARY OF THE INVENTION

[0015] It is an object of the present invention to provide a liquid crystal display having a substrate which is protected against electrostatic charges, regardless of the strength thereof.

[0016] It is another object of the present invention to provide a liquid crystal display which prevents electrostatic charges from entering into the substrate after a shorting bar is removed, thereby minimizing pixel defects.

[0017] It is yet another object of the present invention to provide a manufacturing method of a liquid crystal display in which an LCD panel is prevented from becoming damaged by an electrostatic discharge. while manufacturing costs of the LCD are reduced.

[0018] To achieve the above objects, the present invention provides a liquid crystal display in which a plurality of spark inducing circuits, which extinguish electrostatic charges generated in wires of a TFT substrate, and electrostatic

charging circuits, which charge the electrostatic charges and extinguish the same, are formed on a TFT substrate.

[0019] The spark inducing circuit includes a plurality of the TFTs, connected in series between two adjacent wires and gate electrodes of which are connected to one another; and two capacitors, one electrode of which is connected to the gate electrode of the TFTs and the other electrode of which is connected to the adjacent wire. Since a plurality of the spark inducing circuits are connected in parallel between the adjacent wires, if electrostatic charges generate in the wires, sparks occur in the TFTs of the spark inducing circuits and high voltage current is induced between the source and the drain electrode of the TFTs. This surge current loses its strength by being changed into joule heat. Therefore, the TFTs in an active area are protected from the electrostatic discharge. It is also possible for the electrostatic charges generated in the wires to be dispersed. The spark inducing circuit is formed such that the TFT connects to the capacitor between each wire and a common electrode in series.

[0020] In another aspects, the spark inducing circuit may include a TFT, a gate electrode and a drain electrode of which are respectively connected to the same wire, and a source electrode of which is connected to a dummy line, and a capacitor which is formed between the wire and the drain electrode.

[0021] Meanwhile, a circuit for dispersing electrostatic charges, which comprises a resistor and a capacitor connected in series between a data line and a dummy gate line; and another resistor connected between an adjacent data line of the data line and the capacitor, may be used instead of the spark inducing circuit.

[0022] The electrostatic charging circuit includes a first electrostatic charging circuit, which is formed outside a sealing material by which a TFT substrate and a corresponding substrate are assembled to each other, and a second electrostatic charging circuit, which is formed inside a sealing material. The first electrostatic charging circuit has two capacitors which connect to each other between two adjacent wires in series. A plurality of the first electrostatic charging circuits may be connected to the adjacent wires in parallel. The second electrostatic charging circuit, for preventing electrostatic charges from entering inside the active area, includes capacitors which are formed between each wire and a common electrode. The capacitor includes an additional corresponding electrode connected to the common electrode and the wires. The corresponding electrode which corresponds to the gate line of the wires is made of a metal used for forming the data line, and the corresponding electrode which corresponds to the data line of wires is made of a metal used for forming the gate line. The first and the second electrostatic charging circuits charge and remove the electrostatic charges generating in the wires.

[0023] To protect the TFT substrate from electrostatic charges. a shorting bar, which links all the wires formed on the TFT substrate, is formed inside a cutting line of the substrate. Since the shorting bar remains on the substrate even after the TFT substrate is divided into a plurality LCD panels, it is still possible for the TFT substrate to be protected by the shorting bar.

[0024] To protect the LCD from electrostatic charges occurring in the manufacturing process, a electrostatic discharge protection circuit, a TFT and wires are formed in a substrate, a shorting bar is formed inside the cutting line of the substrate, and the substrate is cut to be divided into several TFT substrates. Next, individual LCD panels are formed and the shorting bar is removed by edge-grinding. After visual display tests are performed by applying test signals to each of the wires, polarizers are attached on the LCD panel on which no defect is detected. Driving circuits are then connected to the LCD panels.

[0025] In the manufacturing method of the LCD, it is possible to protect the LCD panel against electrostatic charges generated during the manufacturing process since the step of cutting the substrate, of injecting liquid crystals and of sealing an injection hole are performed while the shorting bar remains on the LCD panel. Moreover, it is possible to reduce manufacturing costs since polarizers are attached on only the good LCD panels.

[0026] In another embodiment of the present invention, dummy lines are formed outside a visual active area which is defined by a plurality of pixels, the pixels being formed by a plurality of dummy pixels by the intersections of gate and data lines and the dummy lines. A dummy TFT connecting the dummy line is formed in each dummy pixel

[0027] In the above, the ratio of the width to the length of the dummy TFT channel is larger than the ratio of the width to the length of the TFT channel, which is formed in the active area, or one or more dummy TFTs are formed in the dummy pixel. Accordingly, electrostatic charges are dispersed through the dummy TFT when the same is generated.

[0028] A dummy pixel electrode, which is connected to the TFT, is formed in the dummy pixel, and a black matrix which covers the dummy pixel is formed on one of two substrates.

[0029] Generally, since electrostatic charges, which generate at the beginning or end of each step. passes through the dummy gate and data lines which define the dummy pixels surrounding the active area, deterioration caused by electrostatic charges occur in the dummy TFT first. Therefore, the TFTs, which are formed inside the active area and connected to the gate and the data line, are protected against electrostatic charges. Here, damage to the dummy pixels does not affect the quality of the LCD.

[0030] The shape of the dummy TFT may be changed to effectively induce electrostatic charges. It is preferable that the ratio of the width to the area of the dummy TFT channel is bigger than the ratio of the width to the area of the TFT. A plurality of dummy TFTs may be formed in the dummy pixel.

[0031] Meanwhile, a electrostatic charge dispersing pattern, consisting of two electrodes and a semiconductor pattern, is formed outside an active area to discharge electrostatic charges through the channel of the semiconductor pattern. To effectively discharge electrostatic charges, the ends of the electrodes may be pointedly formed and it preferable to form a capacitor in the end of the semiconductor pattern. A plurality of the discharging patterns may be connected to a wire, or two wires, in parallel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] FIG. 1 is a layout view of a conventional liquid crystal display (LCD) substrate which is damaged by an electrostatic discharge;

[0033] FIG. 2 is an enlarged layout view of the thin film transistor in FIG. 1;

[0034] FIG. 3 is a schematic diagram of a LCD substrate according to a preferred embodiment of the present invention;

[0035] FIG. 4 is an enlarged layout view of A in FIG. 3 according to a first preferred embodiment of the present invention;

[0036] FIG. 5 illustrates an equivalent circuit of an electrostatic discharge protection diode circuit shown in FIG. 4;

[0037] FIG. 6 is an enlarged layout view of A in FIG. 3 according to a second preferred embodiment of the present invention;

[0038] FIG. 7 is an equivalent circuit of a first spark inducing circuit in FIGS. 5 and 6;

[0039] FIG. 8 is an equivalent circuit of a second spark inducing circuit in FIGS. 5 and 6;

[0040] FIG. 9 is an equivalent circuit of a third spark inducing circuit in FIGS. 5 and 6;

[0041] FIG. 10 is an equivalent circuit of a fourth spark inducing circuit in FIGS. 5 and 6:

[0042] FIG. 11 is an equivalent circuit of a first electrostatic charging circuit in FIGS. 5 and 6;

[0043] FIG. 12 is an equivalent circuit of a second electrostatic charging circuit in FIGS. 6 and 7;

[0044] FIG. 13 is a layout view of a pattern of the fourth spark inducing circuit of FIG. 10;

[0045] FIG. 14 is a cross sectional view taken along line XIV-XIV' of FIG. 13;

[0046] FIG. 15 is a layout view of another pattern of the fourth spark inducing circuit of FIG. 10.

[0047] FIG. 16 is a cross sectional view taken along line XVI-XVI' of FIG. 15;

[0048] FIG. 17 is a layout view of a dummy pixel for discharging electrostatic charges according to a preferred embodiment of the present invention;

[0049] FIG. 18 is a cross sectional view taken along line XVIII-XVIII' of FIG. 17;

[0050] FIG. 19 is a layout view of a dummy pixel for discharging electrostatic charges according to another preferred embodiment of the present invention;

[0051] FIG. 20 is a layout view of a pattern for discharging electrostatic charges according to a first preferred embodiment of the present invention;

[0052] FIG. 21 is a cross sectional view taken along line XXI-XXI' of FIG. 20;

[0053] FIG. 22 is a perspective view of a capacitor formed in an end of the pattern for discharging electrostatic charges;

[0054] FIG. 23 is a layout view of a pattern for discharging electrostatic charges according to a second preferred embodiment the present invention;

[0055] FIG. 24 is a layout view of a pattern for discharging electrostatic charges according to a third preferred embodiment of the present invention;

[0056] FIG. 25 is a layout view of a pattern for discharging electrostatic charges according to a fourth preferred embodiment of the present invention;

[0057] FIGS. 26A to 26F are cross sectional views used to describe a manufacturing method of the patterns for discharging electrostatic charges of the first to third embodiments of the present invention;

[0058] FIG. 27 is an equivalent circuit of a circuit for preventing electrostatic charges which is connected to a portion of A in FIG. 3 according to a third preferred embodiment of the present invention;

[0059] FIG. 28 is a layout view of the pattern of the circuit in FIG. 27;

[0060] FIG. 29 is a cross sectional view taken along line XXIX-XXIX' of FIG. 28;

[0061] FIG. 30 is a layout view of the pattern of the circuit for preventing an electrostatic discharge which is connected to a portion of A in FIG. 3 according to a fourth preferred embodiment of the present invention;

[0062] FIG. 31 is a cross sectional view taken along line XXXI-XXXI' in FIG. 30;

[0063] FIG. 32 is a layout view of the pattern of the circuit for preventing an electrostatic discharge which is connected to a portion of A in FIG. 3 according to a fifth preferred embodiment of the present invention;

[0064] FIG. 33 is a perspective view of an LCD showing a state in which a thin film transistor substrate and a color filter substrate are assembled to each other; and

[0065] FIG. 34 is a flow chart showing a manufacturing method of an LCD according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0066] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0067] Referring first to FIG. 3, shown is a schematic diagram of a liquid crystal display substrate according to a preferred embodiment of the present invention. As shown in FIG. 3, a plurality of gate lines 100 are formed on a transparent insulating substrate 10 in a horizontal direction, and gate pads 101 are formed at the ends of respective gate lines 100. A plurality of data lines 200 are formed in a

vertical direction to cross the gate lines **100**, and data pads **201** are formed at the ends of respective data lines **200**. Thin film transistors (TFTs), which are switching devices are formed in respect pixel regions PXs defined by intersections of the gate and data lines **100** and **200**. The gathering of a plurality of the pixel regions PX is an active area, confined by an active area line **41**, where the visual image is displayed.

[0068] Shorting bars **102** and **202**, which respectively link all the gate lines **100** and all the data lines **200** at ends thereof, are formed near edges of the substrate **10**. The shorting bars **102** and **202** are interconnected such that the gate and the data lines **100** and **200** are electrically connected. As a result, if electrostatic charges are generated in the gate and data pads **101** and **201**, the electrostatic charges are dispersed through the shorting bars **102** and **202**.

[0069] In the case that the electrostatic charges have a high electric charge value, the electrostatic charges may nevertheless enter into the active area, even with the shorting bars **102** and **202** being provided as described above. In addition, if electrostatic charges are generated after the shorting bars **102** and **202** are removed along a cutting line **11**, the electrostatic charges easily enter the active area. To effectively disperse the electrostatic charges, electrostatic charge dispersing circuits, which are connected to a guard ring or a dummy line **110** surrounding the active area, are provided at an area A of the substrate **10**, i.e., at the area between the pads either **101** or **201** and the active area.

[0070] In a meanwhile, the shorting bars **102** and **202** may be located inside a cutting line **11** of the substrate, differently as illustrated in **FIG. 3**.

[0071] **FIG. 4** shows an enlarged view of the area A in **FIG. 3**. In **FIG. 4**, the cutting line **11**, at which the substrate **10** is cut to remove the shorting bar **102**, a boundary line **21** which corresponds to another substrate **20** oppisite the substrate **10**, and the active area line **41** are shown by dotted lines. The shorting bar **102** is located inside the cutting line **11**, the pads **101** connected to the shorting bar **102** are located between the cutting line **11** and the boundary line **21**, and wires **100** extend from the pads **101** toward the active area. A seal area **90** occupied by a sealant for combing two substrates is located between the boundary line **21** and the active area line **41**. The guard ring or dummy line **110**, made of metal, is placed between the seal area **90** and the active area line **41**, and electrostatic discharge protection diode circuits **120**, spark inducing circuits or electrostatic charging circuits **140** and **150** are connected respective wires **100** and the dummy line **110**.

[0072] Now, the electrostatic discharge protection diode circuits **120** are described with reference to **FIG. 5**.

[0073] A gate electrode and a drain electrode of a TFT Q1 are connected to the dummy line **110**, and a source electrode is connected to the wire **100**. There is provided another TFT Q2 having a gate electrode and a drain electrode connected to the wire **100**, and a source electrode connected to the dummy line **110**. Since the gate and the drain electrodes of the TFTs Q1 and Q2 are connected to each other, the TFTs Q1 and Q2 serves as diodes. As a result, the TFTs Q1 and Q2 are interconnected in a back-to-back mode between the dummy line **110** and the wire **100**.

[0074] The TFTs Q1 and Q2 generally includes an amorphous silicon having high resistance, while the wire **100** is made of a material having tow resistance such as a metal. Therefore, the amount of electrostatic charges which enter the dummy line **110** may be smaller than the amount of electrostatic charges which enter the wire **100**. As a result, it is difficult to completely protect the LCD substrate against electrostatic charges having a large electric charge value using only the circuit shown in **FIG. 5**.

[0075] The spark inducing circuit and the electrostatic charging circuit may help the electrostatic discharge protection.

[0076] As previously mentioned in **FIG. 4**, spark inducing circuits **130** and first electrostatic charging circuits **140** are connected to the adjacent wires **100** at the positions between the seal area **90** and the pads **101**, and second electrostatic charging circuits **150** are connected to the wires **100** at the positions between the seal area **90** and the active area **41**. Therefore, the electrostatic charges are effectively discharged.

[0077] However, since the spark inducing circuits **130** and the electrostatic charging circuits **140** and **150** are located outside the area enclosed by the seal area **90**, circuit defects such as erosion by air or damage by external shocks may occur.

[0078] **FIG. 6** is an enlarged view of the area A in **FIG. 3** according to a second preferred embodiment of the present invention. In the second embodiment, electrostatic discharge protection circuits are located inside the area enclosed by the seal area **90**.

[0079] As shown in **FIG. 6**, spark inducing circuits **130** are connected to wires **100** at the position between the seal area **90** and the active area line **41**, and electrostatic discharge protection diode circuits **120** are connected to the wires **100** as in the previous embodiment. First and second electrostatic charging circuits (not shown) may be provided inside the area enclosed by the seal area **90**.

[0080] A various types of the spark inducing circuits **130** according to the preferred embodiments are shown in FIGS. **7** to **11**. First to fourth spark inducing circuits ST1, ST2, ST3 and ST4 will be described with reference to FIGS. **7** to **10**, respectively, the first to fourth spark inducing circuits ST1, ST2, ST3 and ST4 representing the different types of spark inducing circuits.

[0081] **FIG. 7** illustrates the first spark inducing circuit ST1. As shown in the drawing, the first spark inducing circuit ST1 includes a pair of TFTs Q3 and Q4, which are connected between two adjacent wires **100** in series, and two capacitors C1 and C2. That is, gate electrodes of the TFTs Q3 and Q4 are connected to each other, a source or a drain electrode of one of the TFTs is connected to a source or a drain electrode of the other TFT, and electrodes of the capacitors C1 and C2 are respectively connected to one of the adjacent two wires **10** and to the gate electrodes of the TFTs Q3 and Q4. A plurality of the first spark inducing circuit ST1 are connected to the adjacent two wires **100** in parallel.

[0082] The operation of the first spark inducing circuit ST1 will be described hereinafter. If electrostatic charges generated from the pads **101** enter into the first spark inducing circuit ST1, sparks occur in the TFTs of the first spark inducing circuit ST1 to extinguish the electrostatic

charges. As a result, the TFTs in the active area are protected from the electrostatic charges. In the case that electrostatic charges are generated in the wires **100**, since they are charged in the capacitors C1 and C2 to turn on the TFTs, the electrostatic charges are dispersed through the wires **100**.

[0083] In the first spark inducing circuit ST1, if more than two TFTs are connected between the wires **100** in series, the increase of the current between the wires **100** can be effectively reduced.

[0084] **FIG. 8** shows the second spark inducing circuit ST2. As shown in the drawing, the second spark inducing circuit ST2 includes a TFT Q5 and a capacitor C3. A gate electrode and a drain electrode of the TFT Q5 are electrically connected to each other and a source electrode of the TFT Q5 is connected to the wire **100**. The capacitor C3 is connected between the gate electrode and a common voltage. Vcom which is also connected to a common electrode (not shown). A plurality of the second spark inducing circuits ST1 may be connected to each of the wires **100**.

[0085] In this embodiment, the common electrode is used as a storage electrode, but an additional electrode may be used as the storage electrode.

[0086] **FIG. 9** shows the third spark inducing circuit ST3. As shown in the drawing, the structure of the third spark inducing circuit ST3 is substantially the same as the second spark inducing circuit ST2. However, the third spark inducing circuits ST3 has a plurality of TFTs Q6 and Q7 and only one capacitor C4. The gate electrodes and the drain electrodes of the TFTs Q6 and Q7 are connected to each other and to the capacitor C4, and the source electrodes of the TFTs Q6 and Q7 are connected to the wire **100**. The operation of the third spark inducing circuit ST3 is almost the same as that of the second spark inducing circuit ST2.

[0087] As the same as in the second spark inducing circuit the common electrode is used as a storage electrode, but an additional electrode may be used as the storage electrode.

[0088] The first to the third spark inducing circuits ST1, ST2 and ST3 may be located inside the area enclosed by the seal area **90**.

[0089] **FIG. 10** shows the fourth spark inducing circuit ST4.

[0090] As shown in the drawing, a dummy wire or a guard ring including a dummy gate line **111** and a dummy data line connected to the dummy gate line **111** is provided, and a TFT Q8 is formed on the dummy gate line **111**. A gate, a source and a drain electrodes of the TFT Q8 are connected to the dummy gate line **111**, a data line **200**, and an electrode of a capacitor C5 which has another electrode connected to the dummy gate line **111**.

[0091] In the fourth spark inducing circuit ST4, if electrostatic charges are transmitted to the dummy gate line **111**, the capacitor C5 is charged to turn on the TFT Q8, and the electrostatic charges generated from the dummy gate line **111** and from the dummy data line **112**, are dispersed to the data line **200** and the dummy wires. In the case that the charge value of the electrostatic charges is large, the TFT Q8 is broken down by sparks occurring in the same, thereby extinguishing the electrostatic charges.

[0092] In the first to fourth spark inducing circuits ST1, ST2, ST3 and ST4, the energy due to the electrostatic charges is changed to joule energy by burning the TFTs such that the electrostatic charges do not affect the circuits in the active area.

[0093] **FIG. 11** shows the first electrostatic charging circuit **140** of **FIG. 4**. As shown in the drawing, the first electrostatic charging circuit includes capacitors C6 and C7 which are connected to each other in series between two adjacent wires. A plurality of the circuits are connected to adjacent wires **100** in parallel. The first electrostatic charging circuit may be located outside the area enclosed by the seal area **90**, and it stores electrostatic charges to reduce the level of the same.

[0094] **FIG. 12** shows the second electrostatic charging circuit **150** of **FIG. 4**. Here, the second electrostatic charging circuit finally removes the remaining electrostatic charges so that they do not enter the active area. As shown in the drawing, capacitors a plurality of capacitors C8 are connected between the respective wires **100** and a common electrode voltage Vcom. The second electrostatic charging circuit **150** stores electrostatic charges and reduces the level of the same.

[0095] The fourth spark inducing circuit ST4 of **FIG. 10** will be described in more detail hereinafter with reference to **FIG. 13** illustrating a layout view of the fourth spark inducing circuit ST4 of **FIG. 10**, and **FIG. 14** showing a cross sectional view taken along line XIV-XIV' of **FIG. 13**.

[0096] As shown in **FIGS. 13 and 14**, the fourth spark inducing circuit includes a TFT pattern and a capacitor. The TFT includes a gate electrode which is a portion of a dummy gate line **111**, a gate insulating film **3**, a semiconductor pattern **700** formed on the gate insulating film **3** opposite the gate electrode, a source electrode which is a branch of a data line **200** and a metal pattern **103** serving as a drain electrode. The source and drain electrodes overlap the either edges of the semiconductor pattern **700**. A transparent conductive layer **6** which is connected to the metal pattern **103** and overlaps the dummy gate line **111** to form a storage capacitor. A dummy data line **112** is formed in a vertical direction at the position outer than the fourth spark inducing circuits, and connected to all the dummy gate lines **111** through connecting patterns **5**.

[0097] In detail, a plurality of dummy gate lines **111** are formed on a substrate **10** in a horizontal direction, a gate insulating film **3** is formed thereon, and semiconductor patterns **700** are formed on the gate insulating film **3** opposite the dummy gate line **111**. A dummy data line **112** and a plurality of data lines **200** are formed on the gate insulating film **3** in a vertical direction and the data lines **200** overlap one edges of the semiconductor patterns **700**. A plurality of metal patterns **103**, overlapping the opposite edges of the semiconductor patterns **700** are formed on the gate insulating film **3**, and ohmic contact layers **710** for improving electric contact characteristics are formed between the semiconductor patterns **700** and the data lines **200** and the metal patterns **103**. An interlayer insulating film **4** covers the dummy data line **112**, the data lines **200** and the semiconductor patterns **700**. Contact holes C1 and C3 are pierced in the interlayer insulating film **4**, and contact holes C2 in the gate insulating filme **3** and the interlayer insulating film **4** expose the dummy gate line **111**. Transparent conductive patterns **6** are formed on the interlayer insulating film **4** and connected to the metal pattern **103** through the

contact hole C3, and transparent contact patterns 5 on the interlayer insulating film 4 are connected to the dummy data line 112 and the respective dummy gate lines 111 through the contact holes C1 and C2.

[0098] In this embodiment, it is desirable that the distance between the dummy gate lines 111 is smaller than the distance between the gate lines inside the active area to reduce the area occupied by the dummy wires.

[0099] In the above spark inducing circuit having the TFT and the capacitor structures, when electrostatic charges enter the circuit through the data line 200 or the dummy data line 112, the electrostatic charges charge between the capacitor transparent conductive pattern 700 and the dummy gate line 111, and disappears. The electrostatic charges generating from the dummy data line 200 may be changed into joule heat energy by burning the TFT, and may disappear.

[0100] FIG. 15 is another layout view of the fourth spark inducing circuit, and FIG. 16 is a cross sectional view taken along line XVI-XVI' of FIG. 15, in which an enlarged metal pattern 104 is substituted for the transparent conductive pattern for the capacitor. In this structure, the metal pattern 104 is enlarged to overlap the dummy gate line 111 such that a predetermined storage capacitance is formed between the metal pattern 104 and the dummy gate line 111. The extinguishing of electrostatic charges is performed identically as in the fourth spark inducing circuit ST4 described with reference to FIGS. 13 and 14.

[0101] To prevent electrostatic charges from entering an active area, it is preferable to form dummy pixels having a structure similar with the pixels in the active area.

[0102] FIG. 17 shows a layout view of a dummy pixel for discharging electrostatic charges according to a preferred embodiment of the present invention, and FIG. 18 is a cross sectional view taken along the line XVIII-XVIII' of FIG. 17.

[0103] As shown in the drawings, a gate line or a dummy gate line 100 is formed on the first substrate 10 in a horizontal direction. The portion of the gate line or the dummy gate line 100 functions as a dummy gate electrode. A gate insulating layer film 3 covers the dummy gate line 100, and a dummy amorphous silicon layer 700 is formed on the gate insulating film 3 over the dummy gate electrode. A dummy data line 110 is formed on the gate insulating film 3 in a vertical direction. The dummy gate line 100 and the dummy data line 110 cross each other and define a dummy pixel DP. The dummy pixel may be defined by the crossing of the gate line and the dummy gate line or of the dummy data line and the dummy gate line.

[0104] A dummy source electrode 113, which branches from the dummy data line 110, overlaps an edge of a doped amorphous silicon layer 710, and a dummy drain electrode 114 overlaps another edge of the doped amorphous silicon layer 710 at the opposite side of the dummy source electrode 113. A highly doped amorphous silicon layer 710 is formed at the contact surface of the dummy electrodes 113 and 114 and the dummy amorphous silicon layer 710.

[0105] A width of the dummy source and drain electrodes 113 and 114 is equal to the width of the channel formed in the dummy amorphous silicon 700, and a distance DL between the dummy source electrode 113 and the dummy drain electrode 114 is a channel length DL. Here, the width of the dummy source and drain electrodes 113 and 114 is different from the width of the source and the drain electrode formed in the pixel, and the length between the dummy source electrode 113 and the dummy drain electrode 114 is different from the length between the source and the drain electrode formed in the pixel.

[0106] As described above, to induce electrostatic charges into the dummy pixel, it is preferable that the ratio of the channel width to the channel length in the dummy pixel is more than twice that of the ratio of the channel width to the channel length formed in the active area.

[0107] A passivation film 4 is formed on the dummy data line 110 and the dummy amorphous silicon layer 700, and a contact hole C4 is formed in the passivation film 4 to expose the dummy drain electrode 114. A pixel electrode 300, which is connected to the dummy drain electrode 114 through the contact hole C4, is made of indium-tin-oxide (ITO) on the passivation film 4. The pixel electrode 300 partially overlaps the adjacent dummy gate line 100.

[0108] An alignment film 7 covering the passivation film 4 is formed on the first substrate 10. A black matrix 400, having an opening area at the region corresponding to the dummy pixel DP, is formed on the side of the second substrate 11 facing the first substrate 10. A color filter 500, overlapping the edges of the black matrix 400, is formed in the pixel region DP. Further, a transparent conductive common electrode 600 and an alignment film 8 are, in this order, formed over the color filter 500 and the black matrix.

[0109] Although the black matrix 400 is formed in the second substrate 11 in the LCD according to the present invention, it is possible to form the same in the first substrate 10. In this embodiment, the dummy gate line 100 and the dummy data line 110 are formed outside the active area to prevent electrostatic charges from entering into the active area. In addition, a plurality of the dummy TFTs may be formed in the dummy pixel.

[0110] FIG. 19 is a layout view of a dummy pixel for discharging electrostatic charges according to another preferred embodiment of the present invention. As shown in the drawing, the structure of the discharging dummy pixel is substantially identical to the structure of the dummy pixel shown in FIG. 17, but the dummy gate electrode 101, which is connected to the dummy gate line 100, is extended into the dummy pixel region. Moreover, three (i.e., a plurality) of source electrodes 115, 116 and 117 are connected to the dummy data line 110, and dummy drain electrodes 125, 126 and 127, which respectively correspond to the dummy source electrodes 115, 116 and 117, are connected to the dummy pixel electrode 301 through contact holes C5, C6 and C7.

[0111] A width DW1 of the first dummy source and drain electrodes 115 and 125 is narrower than a width DW2 of the second dummy source and drain electrode 116 and 126, and the width DW2 of the second dummy source and drain electrodes 116 and 126 is narrower than a width DW3 of the third dummy source and drain electrodes 117 and 127. With this structure, all distances DL between the dummy source electrodes 115, 116 and 117 and the dummy drain electrodes 125, 126 and 127 are the same. However, it is possible to form these distances differently.

[0112] Pixel defects in the active area can be prevented by changing the structure of the dummy TFT as described

above and by quickly inducing electrostatic charges to the dummy TFT in the dummy pixel.

[0113] Another discharging pattern for preventing electrostatic charges from entering the active area will be described hereinafter. **FIG. 20** shows a layout view of a electrostatic charge discharging pattern according to a first preferred embodiment of the present invention, **FIG. 21** shows a cross sectional view taken along line XXI-XXI' of **FIG. 20**, and **FIG. 22** is a perspective view of a capacitor which is formed on an end of the electrostatic charge discharging pattern.

[0114] A data line or a dummy data line **110** is formed on a gate insulating film **3** over a substrate **10**, and an amorphous silicon pattern **704** for discharging electrostatic charges is formed on the gate insulating film **3**. The first electrode pattern **118**, which overlaps an edge of the amorphous silicon pattern **704**, is extended from the data line or the dummy data line **110**, and the second electrode pattern **128** overlaps another edge of the amorphous silicon pattern **704** at the opposite side of the first electrode pattern **118**. The ends of the first and the second electrode patterns **118** and **128** are tapered to a point and a doped amorphous silicon pattern **710**, such as an Ohmic contact layer, is formed at the contact surface of the first and the second electrode patterns **118** and **128** and the amorphous silicon pattern **704**. A passivation film **4** is formed over the dummy data line **110**, and the first and the second electrode patterns **118** and **128**; and a contact hole **C8** is formed in the passivation film **4** to expose the second electrode pattern **128**. An ITO pattern **302** for the capacitor is formed on the passivation film **4** and overlaps the second electrode pattern **128**. The ITO pattern **302** for the capacitor is connected to the second electrode pattern **128** through the contact hole **C8**.

[0115] In other words, the discharging pattern includes the amorphous silicon pattern **704**, the ITO pattern **302** for the capacitor for storing electrostatic charges, and the first and the second electrode patterns **118** and **128** which interlink the ITO pattern **302** and the amorphous silicon pattern **704** to the dummy data line **110**. in the LCD having this discharging pattern, electrostatic charges generated in the dummy data line **110** often passes into the ITO pattern **302** through the amorphous silicon pattern **302** and the second electrode pattern **128**, so that the amorphous silicon does not breakdown The reason that the tunneling effect is superior to the breakdown effect is that the first and the second electrode patterns **118** and **128** are pointedly formed so that the electrostatic charges are moved to the ends of the electrode patterns **118** and **128**, rather than to other portions.

[0116] As shown in **FIG. 22**, the ITO pattern **302** of the discharging pattern corresponds to a common electrode **600** of an upper color filter substrate, facing the common electrode. Liquid crystal material LC is interposed between the ITO pattern **302** and the common electrode **600** so that the a storage capacitor Cst is formed in the end portion of the discharging pattern. Since the electrostatic charges moving to the ITO pattern **302** for the capacitor are stored in the storage capacitor, the TFT in the active area is not affected by the electrostatic charges.

[0117] **FIG. 23** shows a layout view of a electrostatic charge discharging pattern according to a second preferred embodiment of the present invention. The structure of the electrostatic charge discharging pattern of the second embodiment is similar to the structure of the electrostatic charge discharging pattern of the first embodiment, but more than two discharging devices are connected to the ITO pattern **302** and the dummy data line **10** in parallel.

[0118] As shown in FIGS. **21** to **23**, the first discharging device, which includes the first amorphous silicon pattern **704** and the first and the second electrode patterns **118** and **128**, and the second discharging device, which includes the second amorphous silicon pattern **705** and the third and the fourth electrode patterns **118** and **129**, are formed on a gate insulating film **3**. The first and the second discharging devices are connected to the dummy data line **110** in parallel. Contact holes **C8** and **C9** to expose the second and the fourth electrode pattern **128** and **129** are made in the passivation film **4**, and the second and the fourth electrode patterns **128** and **129** are connected to the ITO pattern **302** for the capacitor through the contact holes **C8** and **C9**.

[0119] As described in the electrostatic charge discharging pattern of the first embodiment, the ends of the first to the fourth electrode pattern **118**, **128**, **119** and **129** are pointedly formed. The first and the third electrode patterns **118** and **119** respectively face the second and the fourth electrode patterns **128** and **129**. The first and the second patterns **118** and **128** are formed on the first **5** amorphous silicon pattern **704**, and the third and fourth patterns **119** and **129** are formed on the second amorphous silicon pattern **705**. Thus, the electrostatic charges flowing through the dummy data line **110** are discharged to the ITO pattern **302** for the capacitor through the pointed portion and stored in the capacitor. The number of the discharging devices D1 and D2 which are connected to the dummy data line **110** may be increased as required.

[0120] **FIG. 24** shows a layout view of a electrostatic charge discharging pattern according to a third preferred embodiment of the prevent invention. As shown in **FIG. 24**. the second electrode pattern **128** of the first discharging devices D1 and the fourth electrode pattern **129** of the second discharging devices D2 are connected to be adjacent to other data lines **120**. The number of the discharging devices may be increased as required.

[0121] The structures of the electrostatic charge discharging patterns of the first to third embodiments described above have advantages in discharging electrostatic charges generated in the assembly step, the liquid crystal injection step, or the visual test step, since the capacitor is formed after the upper and the lower substrates for the LCD are assembled.

[0122] Referring now to **FIG. 25**, shown is a layout view of a electrostatic charge discharging pattern according to a fourth preferred embodiment of the present invention. As shown in the drawing, the structure of the electrostatic charge discharging pattern of the fourth embodiment is almost the same as that of the first electrostatic charge discharging pattern of the first embodiment, but the dummy metal line **130** is formed on the substrate **10** in a horizontal direction. The dummy metal line **130** is grounded and overlaps the ITO pattern **302** for the capacitor through a gate insulating film and a passivation film. Therefore, a capacitor is formed between the ITO pattern **302** and the dummy metal line **130** for when electrostatic charges move from the first electrode pattern **118** to the second electrode pattern **128** and the ITO pattern **302** by a tunneling effect in the amorphous silicon pattern **704**.

[0123] The electrostatic charge discharging pattern of the fourth embodiment can discharge electrostatic charges more effectively because one more capacitor is formed in the step of forming wires in the substrate.

[0124] Now, a manufacturing method of the electrostatic charge discharging patterns will be described hereinafter with references to FIGS. 21 to 25, and FIGS. 26A to 26F.

[0125] As shown in FIG. 26A, a metal layer for gate wires is deposited on a substrate 10 and patterned to form a gate line and a dummy gate line 100 respectively inside and outside. In the case of the electrostatic charge discharging pattern of the fourth preferred embodiment, a dummy metal line 130 is formed outside an active area in parallel with the gate and the dummy gate line 100 in this step.

[0126] As shown in FIG. 26B, a gate insulating film 3 is deposited with silicon nitride or silicon oxide. Next, an amorphous silicon and a doped amorphous silicon are deposited and then patterned to form an amorphous silicon pattern 704 for discharging electrostatic charges and a doped amorphous silicon layer 710 outside the active area.

[0127] Subsequently, as shown in FIG. 26C, a metal layer for data wires is deposited and patterned to form a data line, a dummy data line 110, the first electrode pattern 118. and the second electrode pattern 128. Where two or more discharging devices are formed, a plurality of pairs of electrode patterns 118, 128, 119, 129 are formed in this step. The doped amorphous silicon material, which is externally exposed, is then removed.

[0128] As shown in FIGS. 26D and 26E, a passivation film 4 is deposited and then the gate insulating film 3 and the passivation film 4 are patterned to form contact holes C8 and C9 to expose the second and the fourth electrode pattern 128 and 129. As shown in FIG. 27F, an ITO is deposited and patterned to form an ITO pattern 302 for a capacitor.

[0129] Next, another circuit for preventing the damage of the substrate by an electrostatic discharge will be described with reference to FIG. 27.

[0130] FIG. 27 is another equivalent circuit of a circuit for preventing electrostatic charges, which is connected to a portion of A in FIG. 3, according to a third preferred embodiment of the present invention.

[0131] As shown in FIG. 27, a first resistor R1 and a capacitor are connected to each other in series between a data line 200 and a dummy gate line 111, and the capacitor and an adjacent data line 200 of the data line 200 are connected in series by a second resistor R2. The dummy gate line 111 is electrically connected to a dummy data line 112 formed outside the data line 200.

[0132] The electrostatic charges generated along the data line 200 passes through the resistors R1 and R2 to disperse in a moment. The electrostatic charges generated to the dummy data line 112 moves along the dummy gate line 111 and stores to the capacitor C1 formed by the data line 200 and the dummy gate fine 111.

[0133] The disappearance of the electrostatic charges will be described with reference to FIGS. 28 and 29.

[0134] FIG. 28 is a layout view of the pattern of the circuit in FIG. 27, and FIG. 29 is a cross sectional view taken along line XXIX-XXIX' of FIG. 28.

[0135] In general, since the device for protecting a substrate from electrostatic charges should be formed in narrow area between an active area and pads, there is a limitation in minimizing the electrostatic charge capacitance by increasing the capacitance of the capacitor. In this embodiment, a semiconductor pattern as a resistance, which connects a capacitor to two adjacent data lines at the same time, is used to increase the ability of dispersing the static electrity.

[0136] As shown in FIGS. 28 and 29, a plurality of gate lines (not shown) are formed on a transparent insulating substrate 10 in a horizontal direction, at least one dummy gate line 11 is formed outside the gate line in the horizontal direction, and a gate insulating film 3 covers the gate lines and the dummy gate line 111.

[0137] On the gate insulating film 3, a plurality of semiconductor pattern 707 and 708 are formed near the dummy gate line 111 with an amorphous silicon material, and a plurality of data lines 200 are formed. Two or more semiconductor patterns 707 and 708 are located between the two adjacent data lines 200. If one of the patterns is named a first semiconductor pattern 707, and the other of the patterns is named a second semiconductor pattern 708, a first electrode 12 connected to the data line 200, and a second electrode 13 facing the first electrode 12 respectively overlap the both sides of the first semiconductor pattern 707. Moreover, a third electrode 15 connected to the other adjacent data line 200, and a fourth electrode 14 facing the third electrode 15 respectively overlap the both sides of the second semiconductor pattern 708. An Ohmic contact layer for improving the contact characteristic intermediates on the surface where the first, the second, the third and the fourth electrodes 12, 13, 15 and 14 contacts the first and the second semiconductors 707 and 708.

[0138] At least one dummy data line 112 is formed outside the data line 200 in parallel with the data line 200.

[0139] A passivation film 4 covers the data lines 200 and the dummy data lines 112, and contact holes C1, C2, C3, and C4, through which the dummy data line 112, the end of the dummy gate line 111, the second and the fourth electrodes 13 and 14 are exposed, are made in the passivation film 4.

[0140] A connecting pattern 5, which overlap the dummy data line 112 and the dummy gate line 111, is formed on the passivation film 4 to connect the dummy data line 112 and the gate line 111. A pattern for a capacitor 9, which overlaps the second and the fourth electrodes 13 and 14 and the dummy gate line 111, is formed to connect the second and the fourth electrodes 13 and 14 though the contact holes C3 and C4. The connecting pattern 5 and the pattern for the capacitor 9 may be made of a transparent indium-tin-oxide (ITO).

[0141] As mentioned above, since the dummy gate line 111 is connected to the dummy data line 112, the electrostatic charges generated along the dummy data line 112 is transmitted to the dummy gate line 111 and is stored between the pattern for the capacitor 9 and the dummy gate line 111 The electrostatic charges generated along the data line 200 loses its energy by passing through the first and the second semiconductor patterns 707 and 708 to be transmitted to the pattern for the capacitor 9, or by demolishing the first and the second semiconductor patterns 707 and 708.

[0142] FIG. 30 is a layout view of the pattern of the circuit for preventing electrostatic charges which is connected to a

portion of A in **FIG. 3** according to a fourth embodiment of the present invention, and **FIG. 31** is a cross sectional view taken along line XXXI-XXXI'**FIG. 30**.

[0143] As shown in **FIGS. 30 and 31**, fifth electrodes **109** are respectively formed under the first and the semiconductor patterns **707** and **708**, so another capacitance is formed between the fifth electrodes **109** and the first and the second semiconductor patterns **707** and **708**.

[0144] The rest structures of the circuit are the same as in the third embodiment.

[0145] **FIG. 32** is a layout view of the circuit for preventing an electrostatic discharge which is connected to A portion in **FIG. 3** according to a fifth preferred embodiment of the present invention, in which dummy gate lines do not cross data lines and comprise a plurality of patterns divided with respect to the data lines

[0146] As shown in **FIG. 32**, each of the patterns of the dummy gate lines **111** is formed along the data line **200** between two the adjacent data lines **200**, and overlaps several capacitor patterns **9** at a time, so sufficient capacitance can be obtained.

[0147] In this embodiment, the dummy gate line **111** is electrically floated.

[0148] Now, a manufacturing method of the LCD, in which damage by an electrostatic discharge can be minimized, will be described hereinafter with reference to **FIGS. 33 and 34**.

[0149] **FIG. 33** shows a perspective view of an LCD showing a state in which a thin film transistor substrate and a color filter substrate are assembled to each other, and **FIG. 34** shows a flow chart showing a manufacturing method of an LCD according to a present invention.

[0150] As shown in **FIGS. 33 and 34**, in STEP **1**, a plurality of wires **100** are formed on a transparent insulating substrate **10**, and a shorting bar **102**, which links all the wires **100** and the pads **101** for contacting with external driving circuits, is formed outside the wires **100**. In this step, electrostatic charge dispersing circuits, such as the diodes, the spark inducing circuits, the electrostatic charging circuits and the discharging patterns. are formed to complete the TFT substrate **10** and a color filter substrate, having a color filter and a common electrode, are formed.

[0151] Next, in STEP **2**, the TFT substrate **10** and the color filter substrate **11** are cut to form each substrate, the substrates **10** and **11** are disposed opposing one another, then liquid crystal material is injected between the substrates **10** and **11**. Electrostatic charges, generating in the step of cutting the substrates **10** and **11** and in the step of injecting the liquid crystal material, are dispersed by the shorting bar **102**.

[0152] In STEP **3**, a hole used to inject the liquid crystal material is sealed and then the shorting bar **102** is removed by a grinding process. In STEP **4**, test signals are applied to each wire **105** to detect defects in the LCD substrate. In this test, it is possible to perform a variety of tests by applying different test signals to each of the wires **100** by using probes which contact to each of the pads **101**. Electrostatic charges generated in this step extinguished in the spark inducing circuits, electrostatic charging circuit, and discharging patterns.

[0153] After the test, STEP **5** is performed. In STEP **5**, polarizers **1** and **2** are attached on outer surfaces of the LCD substrates where there are no defects. In STEP **6**, driving circuits are connected to the pads of the LCD. Generally, electrostatic charges easily generate in the step of attaching the polarizers **1** and **2**. In this method, the electrostatic charges are effectively dispersed by the spark inducing circuit and the electrostatic charging circuit, so that the electrostatic charges can be prevented from entering into the active area.

[0154] Unlike the conventional method, in this manufacturing method of the LCD, since the steps of cutting the substrate, injecting the liquid crystal, and sealing the injection hole are performed with the shorting bar **102** present. the LCD substrate is protected from electrostatic charges generated in the process. In addition, since the polarizers **1** and **2** are attached on substrates which pass the visual test, manufacturing costs are reduced.

[0155] As described above, in the LCD according to the present invention, a dummy line is added outside the active area, a plurality of electrostatic charge dispersing circuits are connected to the dummy line, and the electrostatic charge dispersing circuit is made having a suitable structure to effectively discharge electrostatic charges. Thus, electrostatic charges can be prevented from entering into the active area.

[0156] In addition, since the electrostatic charge dispersing circuits are left remaining after the shorting bar is removed and the expensive polarizers are attached after the visual test, damage to the LCD by an electrostatic discharge is minimized and manufacturing costs are decreased.

[0157] In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purpose of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A liquid crystal display substrate comprising:

a first insulating substrate;

a plurality of pixel electrodes for displaying images provided on the first substrate;

a plurality of switching elements connected to the pixel electrodes;

a plurality of wires farmed on the first substrate and connected to the switching elements; and

a plurality of spark inducing circuits which are connected between the wires adjacent to each other and extinguish electrostatic charges generated on the first substrate by generating sparks responsive to the generated electrostatic charges.

2. A liquid crystal display substrate according to claim 1 further comprising a sealant which is formed on the first substrate and seals the first substrate and a second substrate opposing the first substrate, and wherein the spark inducing circuit is located outside an area enclosed by the sealant.

3. A liquid crystal display substrate according to claim 1 wherein the spark inducing circuit comprises:

a plurality of thin film transistors connected between the adjacent wires in series, and having gate electrodes which are interconnected, and

two capacitors, each having a first electrode connected to the gate electrode, and a second electrode connected to one of the respective wires.

4. A liquid crystal display substrate according to claim 1 wherein the spark inducing circuit comprises:

a thin film transistor having a drain electrode connected to one of the wires, and a gate and a source electrodes connected to each other; and

a capacitors which is connected between the gate electrode of the thin film transistor and a first voltage.

5. A liquid crystal display substrate according to claim 1 wherein the spark inducing circuit comprises:

a plurality of thin film transistors having drain electrodes connected to one of the wires and gate electrodes and source electrodes which are interconnected; and

a capacitor which is connected between the gate electrode and a first voltage.

6. A liquid crystal display substrate according to claim 1, further comprising a first electrostatic charging circuit which is connected between the adjacent two wires and stores and extinguishes electrostatic charges generated in the wires.

7. A liquid crystal display substrate according to claim 6 wherein the first electrostatic charging circuit comprises two capacitors connected to each other in series.

8. A liquid crystal display substrate according to claim 7 further comprising a second electrostatic charging circuit which is connected between the adjacent two wires and in parallel to the first electrostatic charging circuit.

9. A liquid crystal display substrate according to claim 7, further comprising a sealant which is formed on the first substrate and seals the first substrate and a second substrate opposing the first substrate, and wherein the first electrostatic charging circuit is located outside an area enclosed by the sealant.

10. A liquid crystal display substrate according to claim 1 further comprising a sealant which is formed on the first substrate and seals the first substrate and a second substrate opposing the first substrate, and wherein the spark inducing circuit is located inside an area enclosed by the sealant.

11. A liquid crystal display substrate according to claim 10 further comprising a dummy wire formed inside the area enclosed by the sealant, and wherein the spark inducing circuit comprises:

a thin film transistor having a gate electrode connected to the dummy wire and a source electrode connected to the wire. and a drain electrode; and

a capacitor connected between the dummy wire and the drain electrode

12. A liquid crystal display substrate comprising:

a first insulating substrate;

a plurality of pixel electrodes for displaying images provided on the first substrate;

a plurality of switching elements connected to the pixel electrodes;

a plurality of wires which are formed on the first substrate and connected to the switching elements; and

an electrostatic charging circuit connected between the wires adjacent to each other and storing and extinguishing electrostatic charges generated in the wires.

13. A liquid crystal display substrate according to claim 12 wherein the electrostatic charging circuit comprises a capacitor including a first electrode which is a portion of one of the wires and a second electrode.

14. A liquid crystal display substrate according to claim 12 further comprising a sealant which is formed on the first substrate and seals the first substrate and a second substrate opposing the first substrate, and wherein the electrostatic charging circuit is formed located inside an area enclosed by the sealant.

15. A liquid crystal display substrate according to claim 1 further comprising a shorting bar which connects to all the wires and which is formed inside a cutting line of the substrate.

16. A liquid crystal display substrate comprising:

a plurality of gate lines which are formed on a substrate;

a gate insulating film covering the gate lines;

a plurality of data lines which are formed on the gate insulating film and vertically intersect the gate lines;

at least a dummy gate line and a data dummy line which respectively link all the gate lines and all the data lines, the dummy gate line covered with the gate insulating film:

a thin film transistor having a gate electrode which is connected to the dummy gate line, a source electrode which is connected to either the data line or the dummy data line, and a drain electrode: and

a capacitor electrode which is connected to the drain electrode and overlaps the dummy gate line.

17. A liquid crystal display substrate according to claim 16, wherein the capacitor electrode comprises a transparent conductive film connected to the drain electrode through a contact hole in the gate insulating film over the drain electrode.

18. A manufacturing method of a liquid crystal display substrate comprising the steps of:

forming a plurality of liquid crystal display panel regions having thin film transistors, pixel electrodes, wires and electrostatic charge dispersing circuits on a first insulating substrate;

forming shorting bars which link the wires in each of the panel regions;

forming a cutting line for dividing the liquid crystal display panel regions on the first substrate such that the shorting bar is located inside the cutting line;

aligning a second substrate with the first substrate;

sealing the first and the second substrates;

cutting the first substrate along the cutting line to divide into a plurality of liquid crystal display panels;

injecting a liquid crystal material into the liquid crystal display panel through an injection hole,

sealing the injection hole;

removing the shorting bars;

detecting defects in the liquid crystal display panel; and

attaching polarizers on the liquid crystal display panel.

19. A liquid crystal display comprising:

a first insulating substrate;

a plurality of gate lines which are formed on the first substrate;

a plurality of data lines which intersect the gate lines to define a plurality of pixel regions;

a plurality of pixel electrodes which are formed in the pixel regions;

a plurality of first thin film transistors formed in the pixel regions, each thin film transistor includes a gate, a source and a drain electrodes respectively connected to one of the gate lines, one of the data lines and one of the pixel electrodes;

a plurality of dummy data lines which are formed outside an active area including the pixel regions, and intersect the gate lines to define a plurality of first dummy pixel regions;

a plurality of dummy gate lines which are formed outside the active area and intersect the data lines or the dummy data lines to define a plurality of second dummy pixel regions;

a dummy pixel electrode which is formed in the first or the second dummy pixel region;

a dummy thin film transistor which is connected to the gate line, the data line, the dummy gate line and either the dummy data line in the dummy pixel region, and has a ratio of a channel width to a channel length is larger than the first thin film transistors; and

a second substrate which opposes the first substrate.

20. A liquid crystal display according to claim 19, further comprising a black matrix formed on either the first or the second substrate.

21. A liquid crystal display according to claim 20 wherein the dummy pixel electrode is covered with the black matrix.

22. A liquid crystal display according to claim 19 wherein the ratio of the channel width to the channel length of the dummy thin film transistor is more than twice the first thin film transistors.

23. A liquid crystal display comprising:

a first insulating substrate;

a plurality of gate lines which are formed on the first substrate;

a plurality of data lines which intersect the gate lines to define a plurality of pixel regions;

a plurality of pixel electrodes which are formed in the pixel regions;

a plurality of first thin film transistors formed in the pixel regions, each thin film transistor includes a gate, a source and a drain electrodes respectively connected to one of the gate lines, one of the data lines and one of the pixel electrodes;

a plurality of dummy data lines which are formed outside an active area including the pixel regions, and intersect the gate lines to define a plurality of first dummy pixel regions;

a plurality of dummy gate lines which are formed outside the active area and intersect the data lines or the dummy data lines to define a plurality of second dummy pixel regions;

a dummy pixel electrode which is formed in the first or the second dummy pixel region; and

a plurality of dummy thin film transistors which are formed in one of the first or the second dummy pixel regions and are connected to the gate line, the data line, and either the dummy gate line or the dummy data line.

24. A liquid crystal display according to claim 23 wherein the dummy thin film transistors have different values of the ratio of the channel width to the channel length.

25. A liquid crystal display according to claim 23 wherein the dummy thin film transistors are connected to the dummy pixel electrode.

26. A liquid crystal display comprising:

a insulating substrate;

a plurality of wires which are formed on the substrate; and

a first discharging pattern which is connected to one of the wires and has a semiconductor pattern, wherein electrostatic charges are discharged through the channel generated in the semiconductor pattern by tunneling effect.

27. A liquid crystal display according to claim 26 further comprising a storage capacitor formed between the semiconductor pattern and a first voltage.

28. A liquid crystal display according to claim 27 further comprising a plurality of second discharging patterns are connected to the wire in parallel to the first discharging pattern.

29. A liquid crystal display according to claim 28 wherein the first and the second discharging patterns are connected between the adjacent two wires in parallel.

30. A liquid crystal display comprising:

an insulating substrate;

an insulating film which is formed on the substrate;

a wire which is formed on the substrate in a first direction;

an amorphous silicon pattern for discharging electrostatic charges which is formed near the wire;

a first electrode which extends from the wire and contacts an edge of the amorphous silicon pattern; and

a second electrode which contacts another edge of the amorphous silicon pattern, wherein electrostatic charges are discharged from the first electrode to the second electrode through the amorphous silicon pattern by tunneling effect.

31. A liquid crystal display according to claim 30 wherein the ends of the first and the second electrodes are tapered to a point.

32. A liquid crystal display according to claim 31 further comprising:

a passivation film which covers the first and the second electrodes and have a contact hole exposing the second electrode; and

a conductive pattern for a capacitor which is formed on the passivation film and connected to the second electrode through the contact hole, wherein electrostatic charges are stored in a storage capacitor including the conductive pattern and a common electrode formed on a corresponding substrate facing the substrate.

33. A liquid crystal display according to claim 32 further comprising a metal line which is formed on the substrate in a second direction, and overlaps the conductive pattern.

34. A manufacturing method of a liquid crystal display comprising of the steps:

depositing a first metal layer on an insulating substrate;

patterning the first metal layer to form gate wires;

forming a gate insulating film, an amorphous silicon layer, a doped amorphous silicon layer and a amorphous silicon pattern for discharging electrostatic charges;

depositing a second metal layer, and

patterning the second metal layer to form data wires, and first and second electrodes for discharging electrostatic charges connected to the amorphous silicon pattern.

35. A manufacturing method of a liquid crystal display according to claim 34 wherein the first electrode extends from the data wire, the end of the first electrode is pointedly formed, and the pointed end overlaps the edge of the amorphous silicon pattern for the discharge of electrostatic charges.

36. A manufacturing method of a liquid crystal display according to claim 35 wherein the end of the second electrode is pointedly formed and the second electrode overlaps an edge of the amorphous silicon pattern at an opposite side of the first electrode.

37. A manufacturing method of a liquid crystal display according to claim 36, further comprising the steps of:

depositing a passivation film on the data wire and the first and the second electrodes; and

patterning the gate insulating film and the passivation film to form a contact hole exposing the second electrode.

38. A manufacturing method of a liquid crystal display according to claim 37, further comprising the steps of:

depositing a conductive layer; and

patterning the conductive layer to form a pixel electrode and a conductive pattern for a capacitor which is connected to the second electrode through the contact hole.

39. A manufacturing method of a liquid crystal display according to claim 38, further comprising the step of patterning the first metal layer to form a dummy metal line for discharging electrostatic charges.

40. A liquid crystal display having a plurality of pixels comprising:

a plurality of gate lines and a plurality of data lines which intersect each other to define the pixels;

at least one dummy gate line which are formed in parallel with the gate line and located outside an active area which includes the pixels;

a first resistor and a capacitor which are connected in series between a first data line of the data lines and the dummy gate line; and

a second resistor which is connected to the capacitor and to a data line adjacent to the first data line.

41. A liquid crystal display according to claim 40, further comprising at least one dummy data fine which is formed outside the active area in parallel with the data lines, and electrically connected to the dummy gate line.

42. A liquid crystal display comprising:

a plurality of gate lines formed on a substrate;

at least one dummy gate line formed on the substrate outer of the gate lines;

a gate insulating film covering the gate lines and the dummy gate line;

a plurality of data lines which are formed on the gate insulating film and intersect the gate lines and the dummy gate lines;

a plurality of first semiconductor patterns which are formed on the gate insulating film and respectively connected to a first data line of the data lines;

a plurality of second semiconductor patterns which are formed on the gate insulating film and respectively connected to a second data line of the data lines adjacent to the first data line;

a passivation film covering the data lines and the first and the second semiconductor patterns; and

at least one capacitor patterns which are formed on the passivation film, overlap the dummy gate lines and, and are electrically connected to the first and the second semiconductor patterns.

43. A liquid crystal display according to claim 42, further comprising at least one dummy data line which is formed on the substrate in parallel with the data lines and electrically connected to the dummy gate line.

44. A liquid crystal display according to claim 43, further comprising a connecting pattern which is formed on the passivation film, overlaps the end of the dummy gate line and the dummy data line, and is connected to the dummy gate line and the dummy data line through contact holes in the passivation film.

45. A liquid crystal display according to claim 42, wherein the capacitor patterns are located in plural between adjacent two data lines, the dummy gate line comprises a plurality of dummy patterns separated from each other with respect to the data lines, and each of the dummy patterns overlaps the capacitor patterns at a time between adjacent two data lines.

46. A liquid crystal display according to claim 45, wherein the dummy pattern is floated.

47. A liquid crystal display according to claim 42, further comprising a first and a second connecting patterns which are formed on the gate insulating film and respectively connect the first semiconductor pattern to the capacitor pattern and the second semiconductor pattern to the capacitor pattern.

48. A liquid crystal display according to claim 47, wherein the capacitor pattern is made of an indium-tin-oxide.

49. A liquid crystal display according to claim 42, wherein the first and the second semiconductor patterns are made of an amorphous silicon.

50. A liquid crystal display according to claim 42, further comprising electrode patterns which are formed between the substrate and the gate insulating film and located under the first and the second semiconductor patterns.

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